LOW-POWER FREQUENCY SYNTHESIS BASED ON INJECTION LOCKING

MEHRAN M. IZAD

(B.Sc., Iran University of Science and Technology, 2007)

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To my parents

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Contents

Abstract

Low-Power Frequency Synthesis Based on Injection Locking

Mehran M. Izad
Department of Electrical and Computer Engineering
National University of Singapore
Dr. Chun-Huat Heng, Advisor

Advancements in semiconductor industry have empowered consumer devices with higher performance and more functionality with significant reduction in cost due to their ability for mass production. Wireless connectivity has expanded vigorously in these devices. An ever growing demand for higher data transfer rates and lower power consumption has created new challenges on design of these wireless communication systems. Frequency synthesizer is one of the most critical building blocks in RF communication systems which generates carrier signal for transmission. Achieving agility as well as good phase noise with low power consumption has always been a challenge in the design of frequency synthesizers. In this thesis, the concept of injection locking has been used for frequency synthesis in order to increase the power efficiency of the synthesizer and achieve faster settling time. This dissertation is divided into two parts.

In the first part, a low-power ultra wide band synthesizer, as the heart of a high data rate transmitter is designed. Specific emphasis is given on the design techniques to reduce the sidebands while keeping the power consumption low. This is necessary for coexistence of an ultra wide band transmitter with other potentially available standards on the same device. A novel pulse shaping is proposed to suppress the spurious tones and

achieve the required level of spectral purity. Detailed analysis of the effect of circuit non-idealities on the proposed pulse shaping technique is also provided. Moreover, a new approach to estimate the level of spurious tone in injection locked *LC*-oscillators is developed. Finally, a prototype is implemented to demonstrate the feasibility of the idea. Experimental results on the fabricated prototype in 0.13 μm CMOS shows 22 dB of suppression in the spurious tones.

In the second part, a complete ultra low-power high data rate transmitter is designed. New transmitter architecture based on injection-locked ring oscillator and digital power amplifier is proposed. This digitally intensive architecture eliminates the need for slow and power hungry phase locked loop for frequency synthesis and thus increases the power efficiency of the transmitter. Unlike conventional ultra low power radios that trade off spectral efficiency for power efficiency, the proposed architecture adopts spectral efficient 8PSK or O-QPSK modulation to achieve higher data rates. The impact of circuit non-idealities on the transmitter performance are also discussed in depth. Moreover, an analytical expression is derived to estimate the level of spurious tones in injection-locked ring oscillators. To validate the analysis and demonstrate the capability of the proposed architecture, a prototype is fabricated in 65 nm CMOS. Measurements show that the transmitter is capable of achieving a data rate of 55 Mbps while consuming only 853 μW which translate to an energy efficiency of 15.5 pJ/bit.

List of Tables

List of Figures

Chapter 1

Introduction

Advancements in semiconductor industry empowered consumer devices with higher performance and more functionality with significant reduction in cost due to their ability for mass production. Since 1960, the productivity of microchip technology has increased by a factor of one billion times [1]. From the fabrication aspect, the state of the art manufacturing units are able to produce 300mm-Si wafers from a single-crystal ingot of silicon whose body is greater than one meter in length. From the lithography aspect, the printed gate length has been reduced from 25 μm in 1960 to nearly 50 nm in 2009, a 500 times reduction. With all these advancements, digital circuits faithfully obey Moore's law, doubling the number of available transistors every two year.

Analog circuits have also benefited from technology scaling, although at a slower pace due to the many challenges in adapting to degrading device characteristics. Because of the reduction in intrinsic device gain and increase in variability of transistor

parameters, analog building blocks have to adopt higher degrees of design complexity to overcome these impediments. However, the evolution of integrated circuit technology has also brought faster transistors with every new generation; modern CMOS transistors can operate well into the millimeter-wave regime [2]. In terms of radio frequency communication systems, this has created an enormous opportunity for CMOS technology to replace the market previously restricted to more expensive alternatives. Integration capability of CMOS has proved to be a huge advantage. Today transceivers integrate various wireless standards with all analog and digital baseband functions and moves toward system on chip solutions [3]. These devices will deliver an always-on always-aware experience in many ways. They will provide adaptive connectivity, by employing many different radio on the same device, including WiFi, GPS, 3G, 4G, BT, mmWave and, …..In future devices, data rates will be increasing from today's few Mbps to hundreds of Mbps. Within the confinement of the office or house, data rates using wireless local area network will increase from hundreds Mbps to Gbps. Moreover, future devices could be used with body area network to interact with multiple biological sensors over or in body. Therefore, the next generation devices can serve as a link between biological sensor and wide area network to automatically transmit health data and receive required data to make actions on the potentially implanted device on body. These new applications are also providing game changing opportunities for wireless technology [4].

The higher speed, functionality and connectivity have created the exponential growth of energy consumption in mobile devices while there has been only a linear improvement on the lithium battery technology which will likely saturate its energy

density [5]. The result is a major energy gap for portable devices. The goal is a 10x improvement in power of today's devices [6].

In the light of above observations, the goal of this thesis is to identify means for low-power and high-data rate transmitters. Frequency synthesizer is one of the most critical building blocks in transmitters which generates carrier signal for data transmission. Achieving agility as well as good phase noise with low power consumption has always been a challenge in the design of frequency synthesizers. In this thesis, the concept of injection locking has been used for frequency synthesis in order to increase the energy efficiency of the synthesizer and achieve faster settling time. This thesis is divided into two parts.

In the first part, design of a low-power ultra wide band (UWB) synthesizer, as the heart of a high data rate UWB transmitter is explored. Achieving high level of spectral purity in an UWB synthesizer is of great concern as these devices need to coexist with other already available wireless standards. We recognized injection locked based synthesizers as promising substitute for traditional phase locked loops (PLL) for low-power and small area implementation. However, the trade off between hopping time and spectral purity in these circuits is identified as their main limitations. A digital pulse shaping is proposed to address this issue and achieve the required level of sideband suppression for UWB standard. Detailed analysis of the effect of circuit non-idealities on the pulse shaping is also provided. Finally, a prototype is implemented to validate the analysis and demonstrate the feasibility of the idea.

In the second part, ultra-low power high data rate transmitters are investigated. We identified that currently reported ultra-low-power transmitters trade off spectral efficiency to obtain energy efficiency and this limits their data rate to only a few Mbps which is not sufficient for high data rate applications. A new transmitter architecture based on injection locked ring oscillator and digital power amplifier is proposed to address this issue and achieve a transmitter with power consumption of below 1mW with spectral efficient modulations. Circuit design details followed by measured performance of a prototype for this design are provided as well.

1.1 Organization

The main goal of this thesis is to use the concept of injection locking to provide low power solutions for frequency synthesizer in RF transmitters.

In chapter 2, fundamental principles of oscillators in both *LC* and ring oscillators are reviewed. Different phase noise models are provided. A comprehensive theoretical understanding on injection locking in both *LC* and ring oscillators is presented. Geometrical representation of operation of injection-locked oscillators is elaborated and used to obtain their locking range. Several important characteristics of injection locked oscillators such as transient behavior and phase noise are studied to build a foundation for the subsequent chapters.

In chapter 3, system level specification and various frequency synthesizer architectures for ultra wide band were examined. Among them, injection locked based synthesizers are recognized as promising candidates for low-power and small area implementation. However, poor spectral purity and high level of spurious tone in them are identified as their main limitation. A novel pulse shaping technique that reduces the spurious tones is proposed to solve this problem. A new approach to estimate the level of spurious tone in injection locked *LC*-oscillator is also developed. Moreover, mathematical analysis on the achievable spur reduction due to the impact of circuit non-idealities was performed. The detailed implementation of various building blocks in the fabricated prototype is revealed and the experimental results are presented.

In chapter 4, different architectures for ultra-low power transmitters are explored. New transmitter architecture based on injection-locked ring oscillator and digital power amplifier is proposed to increase the data rate and energy efficiency of ultra low power transmitters for biomedical applications. An analytical expression is derived to estimate the level of spurious tones in injection-locked ring oscillators. Furthermore, the impact of circuit non-idealities on the transmitter performance is discussed in depth. CMOS implementation of various building blocks in the fabricated prototype is described and experimental results are provided.

Finally, the conclusion is presented in chapter 5.

Chapter 2

Background

The most commonly used frequency synthesizer in today's transceivers is PLL based synthesizer. However, in order to increase the power efficiency of the synthesizer and achieve faster settling time, this thesis look at the alternative method of frequency synthesis based on injection locking phenomenon in the oscillators. In this chapter, a brief over view of the important characteristics of oscillators under injection is presented to provide a foundation for the subsequent chapters.

2.1 Oscillator Fundamental

In its most basic form, an oscillator is an autonomous circuit that generates a stable periodic output by some self-sustaining mechanism. This is generally achieved by providing a system with a positive feedback such that any loss is compensated and the oscillation can be sustained. This condition, known as Barkhausen's criteria is met if the overall phase around the loop is 2π while the gain is greater than unity at a particular

frequency (oscillation frequency). In this situation, any noise at that frequency is regenerated around the loop and gets amplified until the non-linearity of the system limits the amplitude to a maximum (oscillation amplitude). In this thesis, we use two types of oscillator:

1) Ring oscillators which are based on connecting a series of inverters or amplifiers in series with output of the last stage connect to the input of the first stage. Since only amplifiers or inverters are being used, ring oscillators have the advantage of being fully compatible with the main stream CMOS technology. They are easily scalable with the process and benefit from it. In the modern CMOS technologies, they can oscillate at very high frequencies [7]. Moreover, the area occupied on chip by a ring oscillator is very small and they usually provide a very wide tuning range [8, 9].

2) *LC*-oscillators which are based on tuned circuits (Inductor and capacitor). *LC*-tanks provide infinite amplitude and zero phase shift at resonance frequency. However, inductors in CMOS technology are usually based on spiral inductors fabricated with lossy conductors. Also, due to skin and proximity effects, the series resistance of inductor itself is frequency dependent and becomes significant as frequency increases. Moreover, eddy-currents generated in the substrate flow in opposite direction to that of the coil. This flow of currents in the substrate translates to additional losses [10, 11]. Such an inductor along with lossy capacitor on chips provides finite real impedance at the resonance frequency. Therefore, in order for the oscillator to sustain oscillation at the resonance frequency, a parallel negative resistance needs to be applied to it to cancel out the tank loss. The most

used form of negative resistance is cross-coupled transistors. In summary, *LC*-oscillators consume large area, especially for lower operation frequencies. However, because of their high quality factor (*Q* of *LC*-tank), they offer better phase noise compared to ring oscillators. Their tuning range is also generally limited because of the high *Q* nature of the tank.

2.2 Oscillator Phase Noise

An exact analysis of phase noise in oscillators is mathematically intensive and in many cases provide little design insights. Many solutions for oscillator phase noise [12-18] have been proposed as the research continues to find an accurate closed-form solution that depends only on fundamental device parameters. Typical phase noise plot of an oscillator shows three distinct regions as illustrated in Fig. 2.1. In this section, we briefly touch on some of the models that provide useful design insight in to the above mentioned observation.

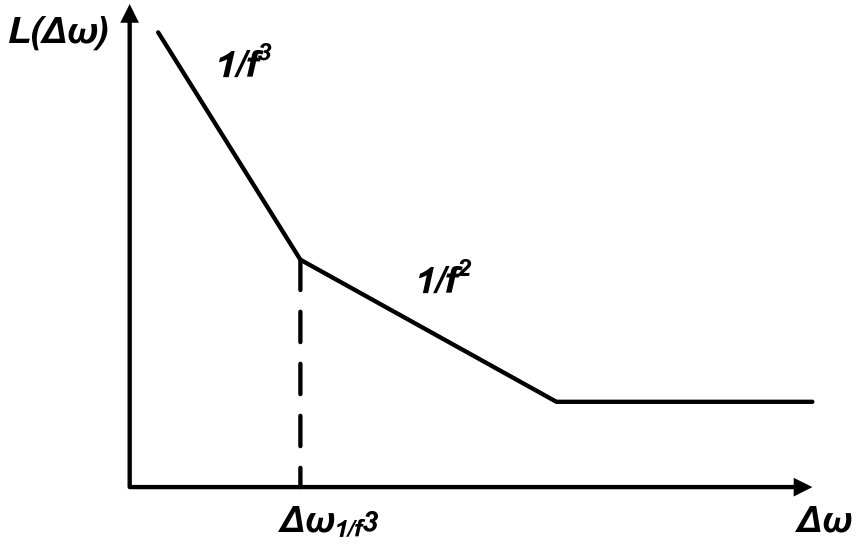


Figure 2.1: Typical phase noise of an oscillator.

Leeson Model: In 1966, Leeson provided a model for the phase noise of *LC* oscillators given by [14]:

$$L(\Delta\omega) = 10\log\left(\frac{2FkT}{P_s}.\left(1+\left(\frac{\omega_0}{2Q\Delta\omega}\right)^2\right).\left(1+\frac{\Delta\omega_{1/f^3}}{|\Delta\omega|}\right)\right) \qquad (2.1)$$

where F is an empirical parameter known as excess noise number, k is Boltzmann's constant, T is the absolute temperature, P_s is the average power dissipated in the resistive part of the tank, ω_0 is the oscillation frequency, Q is the effective quality factor of the tank, $\Delta\omega$ is the offset from the carrier and $\Delta\omega_{1/f^3}$ is the frequency of the corner between $1/f^3$ and $1/f^2$ regions as shown in Fig. 2.1. Although the behavior of $1/f^2$ can be obtained by applying the linear time invariant model and using transfer function approach, the $1/f^3$ portion of the phase noise is completely empirical in this model and has no theoretical basis. Also, excess noise number, F, can only be found through curve fitting using measured data.

Hajimiri Model: In 1998, Hajimiri provided a general model which covers both ring oscillators and *LC*-oscillators [13]. This linear but time varying model naturally accommodates cyclostationary noise sources and their effect on the output phase noise. In particular, it explains the details of how 1/*f* noise in a device up-converts to a close-in phase noise and create the $1/f^3$ portion of the phase noise. However, this technique requires the calculation of an impulse sensitivity function which requires tedious time domain (transient) simulations.

Razavi Model: Since Leeson's model is based on the Q of the resonator tank, ring oscillators could not be analyzed in a similar fashion. In 1996, Razavi proposed a definition of inductor less VCOs that could be used in Leeson's equation to predict their phase noise [16]. The theory can thus be used to mathematically describe the Q of ring oscillators as given by

$$Q = \frac{\omega_0}{2}\sqrt{\left(\frac{dA}{d\omega}\right)^2 + \left(\frac{d\varphi}{d\omega}\right)^2} \qquad (2.2)$$

where A and φ are the gain and the phase of the open-loop transfer function (H) shown in Fig. 2.2.

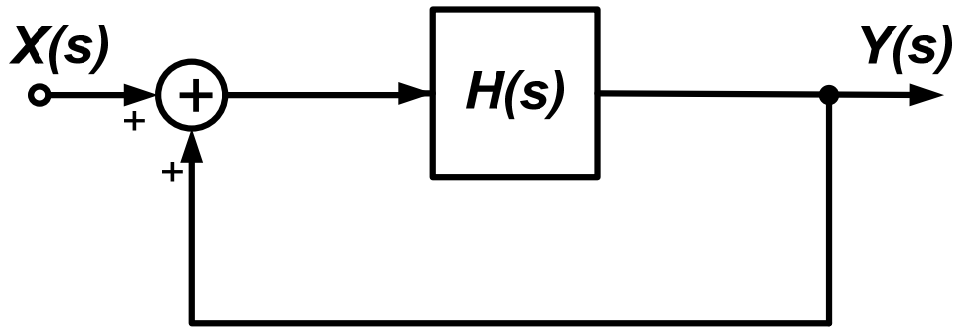


Figure 2.2: Linear model of an oscillator.

Abidi Model: In 2006, Abidi provided analytical closed form expressions for predicting the jitter and phase noise in ring oscillators based on the device parameters [17]. A time-domain jitter calculation method is used to analyze the effects of white noise, while random VCO modulation accounts for flicker noise. This model provides a great insight into design of the ring oscillators, enables manual design for a given specification, and guides for the choice between ring and *LC*-oscillators.

2.3 Injection Locking in Oscillators

Oscillatory systems are important building blocks in variety of fields including optics, mechanics and electronics. Although in principal, an oscillator is an autonomous system which produces output without any input (other than supply), injection of a periodic signal into an oscillator leads to interesting locking or pulling phenomena. As early as 17^{th}, Christian Huygens noticed this behavior in pendulum of the closely spaced clocks on the wall [19]. He postulated that the coupling of mechanical vibration through the wall can cause the pendulums to move in sync.

Synchronization between two oscillators or one oscillator to an injection signal might not happen if the injection power or coupling factor is not enough. In this case injection pulling is observed which is typically undesirable. For example, in an integrated transceiver, the power amplifier output contains large spectral components which can leak through the substrate and the package to the local oscillator on the same chip and causes pulling which severely degrade the performance of the transceiver [19]. On the other hand, injection locking becomes useful in many applications such as clock and data recovery and frequency division and multiplication.

Injection locking in electrical oscillators has been the subject of study from 1927 by Van der pol [20] and many others [19, 21, 22]. By far, the most versatile and powerful expression for the behavior of the oscillators under injection was derived by Adler [23]. In recent years, a generalized form of Adler's equation is presented in [24] which address

some of the simplifying assumption in Adler's analysis and extend it for oscillators coupled to each other with arbitrary strength.

2.3.1 Fundamental Concept

Injection-locking is best understood by analyzing the total phase around the loop of an injection-locked *LC*-oscillator. In this section we first qualitatively discuss the injection locking phenomenon to provide intuitive and geometrical understanding [19, 24]. Next we move to a first order analysis based on [25] which finally reaches to generalized Adler's equation.

Fig. 2.3(a) shows a conceptual oscillator which oscillates at resonant frequency of $\omega_0 = \frac{1}{\sqrt{L_1 C_1}}$. In this oscillator the inverting buffer provides additional 180° phase shift so that total phase shift around the feedback loop is 360°. Now suppose we add a sinusoidal current (at slightly different frequency of ω_{inj}) to the drain current of M_1 (Fig. 2.3(b)). The total vector sum of current that flow through the tank introduce additional phase shift of φ around the loop (Fig. 2.3(c)). Thus, the oscillation frequency must change such that the tank contributes enough phase shift to cancel the effect of φ as shown in Fig. 2.3(d)). If the amplitude and frequency of I_{inj} are chosen properly, indeed oscillator oscillates at ω_{inj} and we say oscillator is injection locked to the I_{inj}. We can see that for this to happen, the angle between the total tank current and the tank voltage (in-phase with I_{osc}) must be equal to the angle of impedance at the injection frequency. From

geometry, we can see that the solution exist if the line OA at angle φ with the horizontal line intersects a circle of radius I_{inj} (Fig. 2.3(c)). This requires

$$I_{inj} > I_{osc} \sin\varphi \qquad (2.3)$$

and φ relates to the circuit elements as

$$\tan\varphi = R(C_1\omega_{inj} - \frac{1}{L_1\omega_{inj}}) \approx \frac{2Q}{\omega_0}\Delta\omega \qquad (2.4)$$

where $\Delta\omega = \omega_{inj} - \omega_0$. Thus, the oscillator locks when

$$\frac{I_{inj}}{I_{osc}} > \frac{|\Delta\omega|}{\sqrt{\Delta\omega^2 + \frac{\omega_0}{2Q}}} \qquad (2.5)$$

Therefore it remains lock over the one-sided locking range of

$$\omega_L = \frac{\omega_0}{2Q}\frac{I_{inj}}{I_{osc}}\frac{1}{\sqrt{1-\left(\frac{I_{inj}}{I_{osc}}\right)^2}} \qquad (2.6)$$

With the foregoing observations in mind, we can now consider a more general oscillator under injection. Here we adopt injection locked oscillator (ILO) model shown in Fig.2.4 for any injection method and oscillator topology [22, 26]. H_{VCO} is the voltage controlled oscillator small signal open loop frequency response and will depend on VCO topology. For *LC* VCOs, H_{VCO} is the tank frequency response whereas for ring oscillators, it is a low pass response. We assume the free running oscillation frequency is ω_0 and we use phasor diagram shown in Fig. 2.3(c). We will take I_{inj} as reference. Assuming that instantaneous oscillation frequency is ω, the oscillator output phasor $I_{osc} = |I_{osc}|e^{j\theta}$ rotates with instantaneous angular frequency of $\frac{d\theta}{dt} = \omega - \omega_{inj}$.

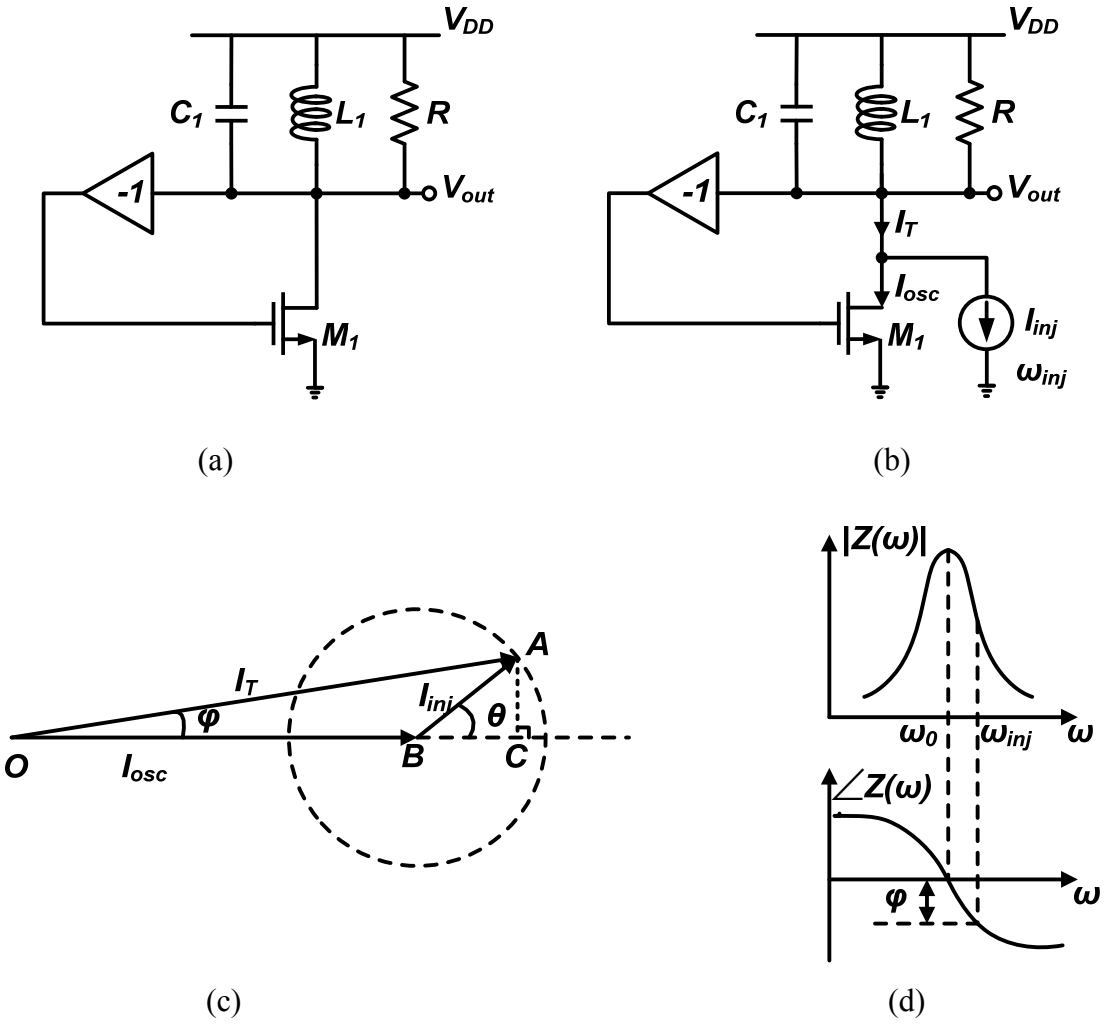


Figure 2.3: (a) Conceptual oscillator. (b) Frequency shift by injection. (c) Geometrical interpretation. (d) Tank characteristic.

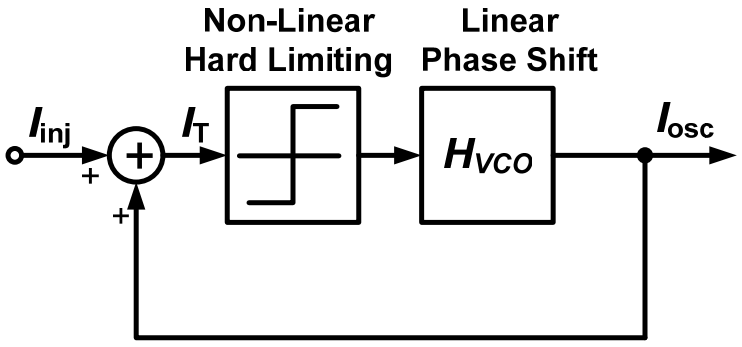


Figure 2.4: ILO Model in [22, 26].

The phasor I_T is vector summation of I_{inj} and $I_{osc;}$ $I_T = I_{osc} + I_{inj} = |I_T| e^{j(\theta-\varphi)}$ where φ is the phase shift introduced by the H_{VCO} to satisfy the oscillation condition, $\varphi = \angle H_{VCO}$. As can be seen in Fig. 2.3(c),

$$\sin\theta = \frac{\overline{AC}}{I_{inj}}, \quad \cos\theta = \frac{\overline{BC}}{I_{inj}} \tag{2.7}$$

From geometry and (2.7)

$$\tan\varphi = \frac{\overline{AC}}{\overline{OA}} = \frac{\overline{AC}}{I_{osc} + \overline{BC}} = \frac{K\sin\theta}{1 + K\cos\theta} \tag{2.8}$$

where $K = I_{inj} / I_{osc}$. We define [25],

$$A \equiv \frac{\tan\varphi}{\omega_0 - \omega} \tag{2.9}$$

We know that $\omega - \omega_{inj} = \frac{d\theta}{dt}$, thus

$$\tan\varphi = -A\left(\frac{d\theta}{dt} - (\omega_0 - \omega_{inj})\right) \tag{2.10}$$

Equating $\tan\varphi$ from (2.8) and (2.10),

$$\frac{d\theta}{dt} = -\frac{1}{A}\frac{K\sin\theta}{1 + K\cos\theta} + (\omega_0 - \omega_{inj}) \tag{2.11}$$

This is the same locking equation as Adler's but generalized for any topology and any level of injection. For a parallel RLC tank [22, 23],

$$A = \frac{2Q}{\omega_0}. \tag{2.12}$$

In order to find the value of A for ring oscillators, we simplify (2.9) by taking the first order expansion of $\tan\varphi$ around $\omega = \omega_0$,

$$A \approx -\left.\frac{d\tan\varphi}{d\omega}\right|_{\omega=\omega_0} \tag{2.13}$$

We assume that the ring oscillator is implemented with *N* identical stages with a low pass transfer function of

$$H_{VCO}(j\omega) = \frac{H_0^N}{(1 + j\frac{\omega}{\omega_p})^N} \qquad (2.14)$$

Since the positive feed back introduce 180° phase shift,

$$\varphi\big|_{\omega=\omega_0} = \angle H_{VCO} = -N\tan^{-1}(\frac{\omega_0}{\omega_p}) = -\pi \qquad (2.15)$$

From (2.14)and (2.15),

$$H_{VCO}(j\omega) = \frac{H_0^N}{(1 + j\frac{\omega}{\omega_0}\tan(\frac{\pi}{N}))^N} \qquad (2.16)$$

$$\varphi = -N\tan^{-1}(\frac{\omega}{\omega_0}\tan(\frac{\pi}{N})) \qquad (2.17)$$

Using approximation in (2.13),

$$A \approx -\frac{d\tan\varphi}{d\omega}\bigg|_{\omega=\omega_0} = \frac{N}{\omega_0}\frac{\tan(\frac{\pi}{N})}{\sec^2(\frac{\pi}{N})}\sec^2\varphi\big|_{\omega=\omega_0} = \frac{N}{\omega_0}\frac{\tan(\frac{\pi}{N})}{\sec^2(\frac{\pi}{N})} = \frac{N}{2\omega_0}\sin(\frac{2\pi}{N}) \qquad (2.18)$$

Note that the accuracy of (2.18) diminishes as the difference between free running frequency and injection frequency increases.

If the oscillator locks to the injection signal, its frequency will always track the input frequency and therefore, $\frac{d\theta}{dt} = 0$. Making this substitution to (2.11),

$$\omega_0 - \omega_{inj} = -\frac{1}{A}\frac{K\sin\theta_{ss}}{1 + K\cos\theta_{ss}} \qquad (2.19)$$

where θ_{ss} is the steady sate phase shift between injected and output signals. The maximum value of the deviation of injection frequency from free running is obtained when $\cos\theta_{ss} = -K$. Hence we can find lock range by

$$\omega_L = \frac{1}{A}\frac{K}{\sqrt{1-K^2}} \qquad (2.20)$$

For small injection strength, we can find the simplified steady state phase difference by

$$\theta_{ss} \approx \sin^{-1}\left(\frac{A}{K}(\omega_0 - \omega_{inj})\right) \qquad (2.21)$$

Note that the above analysis is based on phasors and transfer functions which is true for non-harmonic oscillators (like ring oscillators) as long as the large signal behavior of the building blocks is close to their small-signal response and they operate quasi-linearly. If the oscillator is operating in strong non-linear regime, the model above does not apply but time-domain model presented in [27] can be used. Let us solve this case for the most practical circuit of ring oscillator that consists of a differential pair with *RC* loads as the delay cell. In strong non-linear mode, the differential pair acts like a comparator, and provide a step like current with amplitude I_{BIAS} to the load (total tail current of the differential pair). The step response of the *RC* circuit with this step current is an exponential waveform. With no injection, and assuming an *N*-stage ring oscillator, the period of oscillation is $2Nt_d$ where t_d is the delay contributed by each stage. With the exponential waveforms as shown in Fig. 2.5, the addition of injection signal with delay Δ compared with oscillator signal leads to an additional delay *d* in the stage that injection happens. Thus the oscillator can now oscillate with period $2Nt_d+d$. This extra delay is calculated in [27]:

$$d(\Delta) = RC\ln(\frac{V_{a,\max} + V_a + (V_{ainj,\max} + V_{ainj}).e^{\frac{\Delta}{RC}}}{V_{a,\max} + V_a + V_{ainj,\max} + V_{ainj}}) \quad (2.22)$$

where V_a is the oscillation amplitude, $V_{a,\max} = I_{BIAS}R$, V_{ainj} is the injection amplitude and $V_{ainj,\max}$ is the maximum injection amplitude depends on the tail current of the injection differential pair. The lock range can thus be estimated by calculating the minimum and maximum delay that is possible by particular injection strength. It can be shown [27] that the oscillator remains locked if

$$T + 2d_{\min} < T_{inj} < T + 2d_{\max} \quad (2.23)$$

where,

$$d_{\max} = d(\Delta_{\max}) = RC\ln(\frac{V_{a,\max}}{V_{a,\max} - V_{ainj}}) \quad (2.24)$$

$$d_{\min} = d(\Delta_{\min}) = RC\ln(\frac{V_{a,\max}}{V_{a,\max} + V_{ainj}}) \quad (2.25)$$

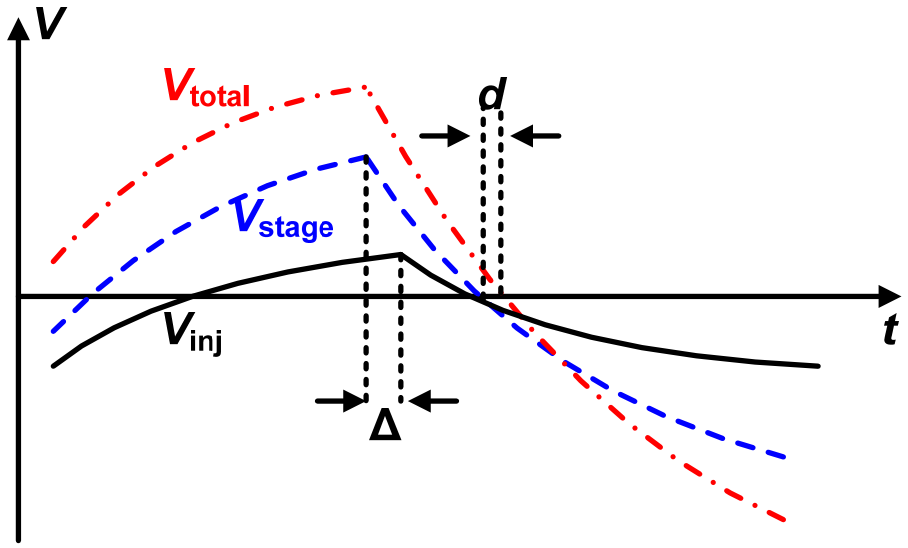


Figure 2.5: Effect of injection on the output voltage V_{total}=V_{stage}+V_{inj}.

Note that the above analysis shows that the entire loop delay is changed by changing the delay of just one delay cell. This can create phase imbalance in the applications that use ring oscillators as multi phase generator. It also leads to lower locking range. These issues can be addressed by multiple injections into the loops to change the delay of all the stages at the same time [28, 29]. However, such a technique requires proper progressive phases for injection which is not always easy. Possible solutions are using a replica delay line [30] or progressive injection locking [31].

2.3.2 Phase Noise

The phase noise of oscillators can be reduced by injection locking to a low-noise reference signal. We first analyze the phase noise mathematically based on the model in [19]. Next we provide an explanation in time domain based on the concept of realigned oscillators.

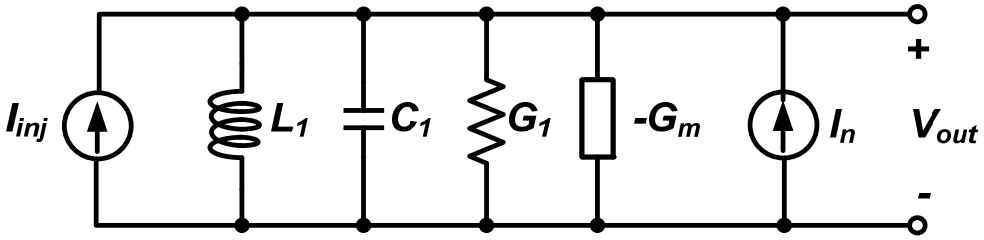


Figure 2.6: Model of *LC*-oscillator for phase noise study.

Fig. 2.6 shows the model of an *LC* oscillator under injection. The noise of the tank and $-G_m$ Cell are shown as a current source I_n. In the absence of injection, the average value of $-G_m$ cancels the losses G_1 and I_n goes through the following transfer function:

$$\frac{V_{out}}{I_n} \approx \frac{1}{|2(\omega_n - \omega_0)C_1|} \qquad (2.26)$$

Therefore, noise is amplified by a huge gain as the noise frequency gets closer to the oscillation frequency. When an injection source with frequency close to free running frequency exist, the average value of $-G_m$ changes as shown in Fig. 2.7.

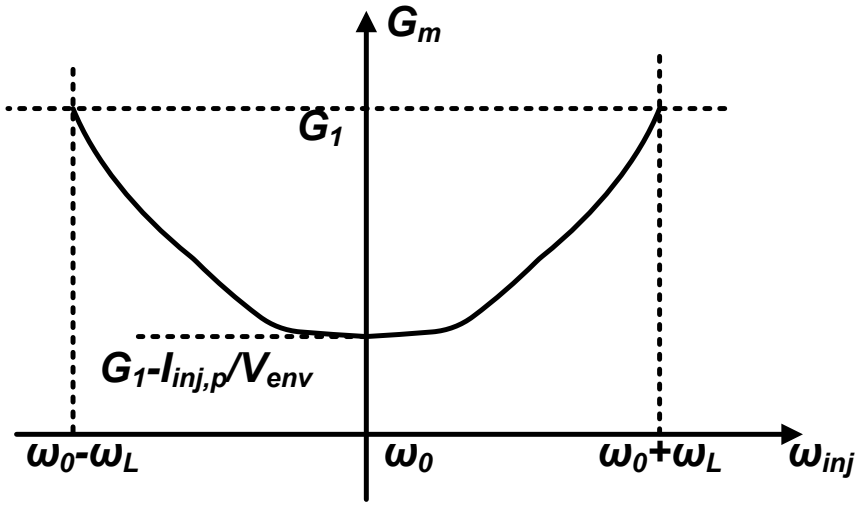


Figure 2.7: Variation of *Gm* across the lock range.

It is shown in [19] that the overall tank impedance rises to $G_1 - G_m = I_{inj,p} / V_{env,p}$, where V_{env} is the envelope of the output V_{out}. This observation shows that the tank impedance at frequencies close to ω_0 falls from almost infinity to $I_{inj,p} / V_{env,p}$. Thus the noise is less amplified and the phase noise is reduced. As can be seen in Fig. 2.7, this change in impedance diminishes as the injection frequency deviates from the free running frequency. Therefore, the locked and free running phase noise profiles meet at the edge of the lock range. Using the general analysis in section 2.4.1, it has been shown in [25] that input phase noise is low-pass filtered with transfer function of

$$JTF_{input} = \frac{1}{1+\frac{j\omega_n}{\omega_P}} \qquad (2.27)$$

and the oscillator phase noise is high pass filtered with transfer function of

$$JTF_{VCO} = \frac{\frac{j\omega_n}{\omega_P}}{1+\frac{j\omega_n}{\omega_P}} \qquad (2.28)$$

where $\omega_P = \sqrt{\frac{K^2}{A^2} - (\omega_0 - \omega_{inj})^2}$.

From the time domain perspective, jitter in a free running oscillator accumulates over time, resulting in a drift of the phase in time which is referred as phase noise in frequency domain. Injection locking corrects the zero crossing of the oscillator in every period, thereby truncating the jitter accumulating process and lowering the phase noise.

2.3.3 Transient behavior

Transient behavior of an injection locked oscillator can be obtained by solving the Adler's equation. Traditional solution for low level injection is given by [23],

$$\tan(\frac{\theta}{2}) = \frac{\omega_L}{\omega_0 - \omega_{inj}} - \frac{\omega_B}{\omega_0 - \omega_{inj}} \tanh(\frac{\omega_B (t - t_0)}{2}) \qquad (2.29)$$

where $\omega_B = \sqrt{\omega_L^2 - (\omega_0 - \omega_{inj})^2}$ and t_0 is an integration constant. This solution can be used to directly calculate the phase lock time of the oscillator. However, this equation is complicated and provides little design insight. With the assumption that the difference

between initial and steady state phase of the oscillator output is smaller than π and the injection frequency is close to free running frequency, (2.29) can be simplified to [32]

$$\theta(t) = \theta_{ss} + (\theta(0) - \theta_{ss})e^{-\omega_L t} \qquad (2.30)$$

The corresponding frequency settling behavior of oscillator is given by

$$\omega(t) = \omega_{inj} + \omega_L(\theta_{ss} - \theta(0))e^{-\omega_L t} = \omega_{inj} + \omega_L(\theta_{ss} - \theta(0))e^{-\frac{t}{\tau}} \qquad (2.31)$$

(2.31) shows several interesting characteristic of ILOs.

First, we observe that if the initial and steady-state phase of the oscillator are close to each other ($\theta_{ss} \approx \theta(0)$), instantaneous or very short frequency settling time is achievable. This can be a method to obtain fast locking in ILOs. In many applications, it is required to hop between two known frequencies (e.g. $\omega_{inj,1}, \omega_{inj,2}$). Neglecting the initial phase at startup, the steady state phase of oscillator output at one frequency is the initial phase for the next jump. Therefore, the above mentioned condition can be obtained if $\theta_{ss1} \approx \theta_{ss2}$ or equivalently using (2.21)

$$\frac{\omega_{0,1} - \omega_{inj,1}}{\omega_{L,1}} \approx \frac{\omega_{0,2} - \omega_{inj,2}}{\omega_{L,2}} \qquad (2.32)$$

(2.32) can be realized if we can control the free running frequency of the oscillator with such a fine resolution that the difference between ω_0 and ω_{inj} in any case is very small. However, frequency control with such a fine resolution might be non-trivial.

Second, (2.31) shows a first-order settling behavior. Assuming a 4τ settling time, we can conclude that in any case of initial and steady-state phase difference, the oscillator can settle with lock time of

$$t_{lock} \approx 4\tau = \frac{4}{\omega_L} \qquad (2.33)$$

Therefore, increasing the lock range can reduce the lock time of the oscillator. By proper choice of lock range one can achieve a very fast frequency synthesizer using ILOs [33, 34].

2.4 Chapter Summary

In this chapter, a brief background of oscillators is presented and different phase noise models for both *LC* and ring oscillators are reviewed. Next, an analytical framework is developed to describe the behavior of an oscillator under injection of a periodic signal. Characteristics of injection locked oscillators are discussed and a graphical interpretation is presented. A mathematical model of injection locked oscillators is derived and phase noise reduction property is studied in detail. Transient behavior of injection locked oscillators based on the Adler's equation is described and different techniques to achieve fast-locking are introduced.

Chapter 3

Low-Spur Fast-Hopping Frequency Synthesizer Based on Injection Locking

3.1 Introduction

In Chapter 2, a complete understanding of an oscillator under injection was established. A mathematical model for the injection locked oscillator was derived which can predict the locking range and transient behavior of the oscillator. However, the discussion was about a single tone input. When a multi-tone input is injected, the oscillator locks to the tone which is within the lock range. This happens when input signal has rich harmonic content like a square wave. This phenomenon is called sub-harmonic injection locking. The locking range and the transient behavior is similar to the fundamental locking, but the injection strength and frequency in this case is determined by the frequency and power of the injection signal at that particular input harmonic. Thus, the oscillator will lock to the N^{th} harmonic of an injection signal if the free running

frequency of the oscillator is close to that harmonic. This sub-harmonic locking causes the oscillator output frequency to become N times the injection signal frequency. In fact, a sub-harmonic injection-locked system acts like an integer-N frequency synthesizer without a need for any phase detector, divider and loop filter. We also showed in chapter 2 that when the oscillator is under injection locking, the phase noise within locking range will be suppressed to that of the injection signal. It could thus be deduced that for a sub-harmonic locking with frequency ratio N, the phase noise within locking range would be constrained to $\mathcal{L}_{inj}+20\log N$, where $\mathcal{L}_{inj}$ is the phase noise of the sub-rate injection signal. Therefore, a sub-harmonic injection locked oscillator can provide a compact, low-power and low-phase noise solution for frequency synthesis with fast transient response.

In sub-harmonic ILOs, the injection signal is usually a train of pulses generated from a reference signal. Square wave pulses are rich in harmonic content and provide more power for injection at higher order harmonics. However, only one of the harmonics locks the oscillator while the others, whose frequencies are out of the locking range appear at the output with limited suppression. These unwanted harmonic spurs at the output are especially harmful in wide-band systems such as software defined radio and Ultra Wide Band (UWB) where strong interferers from other standards are expected. In this chapter, this issue is addressed by proposing a pulse shaping technique that reduces the unwanted harmonics in the injection signal and produces low-spur synthesized output. To validate the effectiveness of the proposed technique, a test chip tailored to the first band group of WiMedia-UWB is fabricated and the measurement results are provided.

3.2 Wi-Media UWB System Specification

In 2002, the FCC opened up unlicensed spectrum between 3.1 to 10 GHz for UWB communication applications. The WiMedia standard for UWB is based on subdivision of the large available bandwidth into sub bands of 528 MHz each (Fig. 3.1). The center frequency of each sub band is at odd harmonic of 264 MHz.

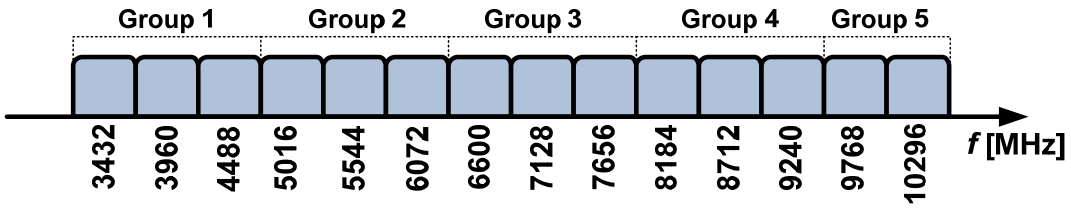


Figure 3.1: Frequency allocation of WiMedia UWB.

Three sub-bands are grouped together in a band group, except for band group 5, which consists of two sub-bands only. Band group 1 is the mandatory mode of operation and spans from 3168 to 4752 MHz. The applied data mapping onto a complex constellation is QPSK for data rates up to 200 Mbps and dual carrier modulation (DCM) for data rates from 320 Mbps and higher. An orthogonal frequency division multiplexing (OFDM) technique using 128 subcarriers is applied to generate the discrete-time signal. Out of these 128 subcarriers, 100 carriers are used for data, 22 carriers are pilot tones, and the remaining carriers are null tones. A frequency-hopping (FH) scheme is implemented within each of the band groups, but not across band groups. The permitted band-switching time is only 9.5 ns in all cases, whereas the symbol period is 312.5 ns.

An important consideration is the treatment of interference. The transmit levels of different systems that generate interference needs to be considered carefully. The WiMedia UWB interference scenario recommendation is depicted in Fig. 3.2 [35].

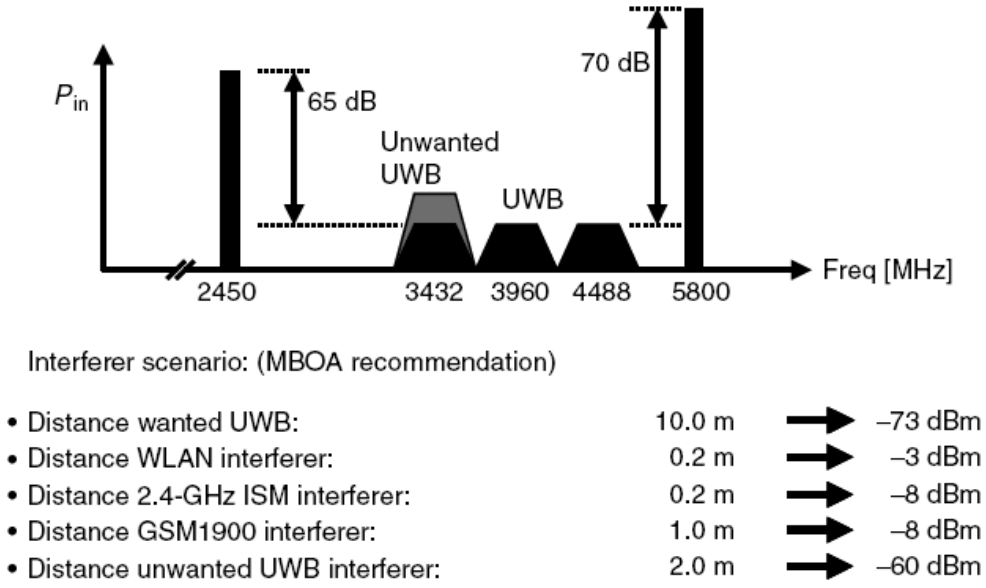


Figure 3.2: WiMedia interference scenario.

A wanted UWB transmitter is located at a distance of 10-m from the UWB receiver. The received transmit power S at the antenna reference point (ARP) of the UWB receiver operating in sub-band 1 is −73 dBm, according to

$$S = \frac{1}{4\pi r^2} \cdot \frac{\lambda^2}{4\pi} \cdot P_{TX} \qquad (3.1)$$

where r is the distance in meters, λ is the wavelength in meters, and P_{TX} is the transmit power which is −10.3 dBm for an UWB signal. Here, a free-space loss is assumed. According to the interferer scenario, an unwanted UWB transmitter may be as close as 2-m and if this transmitter operates in sub-band 2, the received transmit power at the ARP

is −60 dBm, which is 13 dB stronger than the wanted UWB signal. From the proposed interferer scenario and resulting power levels (Fig. 3.2), we observe that there can be a power difference of as much as 70 dB between the wanted signal and the interferer. Even with an antenna filter in front of the radio, this will set very stringent linearity requirements.

3.2.1 Synthesizer Requirement

As the WiMedia-UWB radio must cover at least the lower three bands, and since a zero-IF architecture is most likely to be used, the synthesizer needs to provide quadrature carrier signals at the center frequencies of the mandatory sub bands (band group 1). The requirements on in-phase and quadrature phase (*I*/*Q*) mismatch are relaxed and up to 6° phase and 0.6 dB gain mismatch is tolerable [36].

As mentioned before, a FH scheme is implemented within each of band group, but not across band groups. The permitted band-switching time is only 9.5 ns in all cases. Therefore, the synthesizer must be able to perform a frequency hop and settle to the new frequency within 9.5 ns, which is a challenging requirement.

The demands on the spectral purity of the generated carriers are stringent due to the presence of strong interferer signals. The spur requirement can be calculated from the interferer scenario according to

$$Spur(dBc@offsetFrequency) = P_{PSD-wanted} - P_{PSD-\text{int}erfierer} - SNR \qquad (3.2)$$

where PSD represents the power spectral density (in dBm/MHz). Following the interferer scenario and associated received power levels of the interferers, all spurious tones in the 5 GHz range must be below −50 dBc. This spur-level requirement will avoid harmful down-conversion of strong out of band WLAN interferers into the wanted sub-bands. For the same reason, the spurious tones in the 2.4 GHz range should be below −45 dBc to allow coexistence with the systems operating in the 2.4 GHz ISM band, such as IEEE802.11b/g and Bluetooth. The requirements for in-band spurious tones can be calculated in a similar way. The specified spurious tone level is −35 dBc [37].

Another particular important measure of the synthesizer is the maximum tolerable phase noise. In order to quantify the effect of phase noise on the constellation, system level simulation needs to be done. It has been shown in [37] that the overall integrated phase noise from DC to 50 MHz should not exceed 2° rms. This can be recalculated to a phase noise requirement of −100 dBc/Hz at 1 MHz offset from the carrier.

3.3 Existing UWB Synthesizers

As discussed in the previous section, the band switching must occur within 9.5 ns. Classical integer-N PLLs are usually ill-suited for fast hopping systems. This is primarily because the bandwidth requirement for such settling times is large. However, in a typical charge-pump-based PLL, the loop bandwidth is constrained by the input reference due to stability issues. (The bandwidth has to be approximately ten times smaller than the reference frequency [38]). Several alternative architectures have been proposed to achieve the required band switching time which will be discussed here.

3.3.1 Integer-*N* PLLs

If only mandatory bands need to be generated, one can use 3 PLLs. Each PLL generates one of the three required carrier frequencies. A high-speed three-to-one multiplexer can select the intended LO signal. This option is only practical in those cases where *RC* ring oscillators can fulfill the requirements. Three *LC*-oscillator-based PLLs will incur huge area penalty. The option of using ring oscillators has been considered in [36]. The use of a 66 MHz reference frequency allows a loop bandwidth of about 5 MHz, thus suppressing the close-in phase noise of the oscillators considerably. However, due to proximity of these frequencies, pulling via substrate might be a severe issue.

3.3.2 Two PLLs and SSB Mixers

Two PLLs along with SSB mixers were used in early approaches. Generally, one of the PLLs will generate the center frequency of the targeted band whereas the other PLL will generate the desired offset frequency. Frequency pulling via substrate is mitigated in this case because of the larger difference between the two PLL's frequencies. By employing a SSB mixer, this architecture can cover the desired output frequencies through frequency addition or subtraction [39-41]. Different architectures have been used for generating the desired frequency based on the above concept. In this approach, PLLs usually operate at twice of the desired frequency in order to create quadrature output using a divide by-2 circuit. Some architectures, such as [41], requires the use of dividers with sophisticated dividing ratios. Generation of quadrature signals at the output of these dividers is a major issue. Moreover, the unintentional spurious tones (closed to the interferers) generated by the non-linear mixing action might degrade the overall receiver

sensitivity. For example, one can generate the center frequency of band group2 (3960 MHz) and the required frequency spacing of 528 MHz using 2 PLLs. In this realization, the third harmonic of the 528 MHz signal (at 1584 MHz) is particularly troublesome because after mixing with 3960 MHz, this harmonic will cause a spurious tone at either 3960 MHz + 1584 MHz = 5544 MHz or 3960 MHz − 1584 MHz =2376 MHz. Both spurious tones are close to possible strong interferer signals (5 GHz and 2.4 GHz ISM bands, respectively). Fig 3.3 shows a typical SSB approach spectrum along with spurious tones.

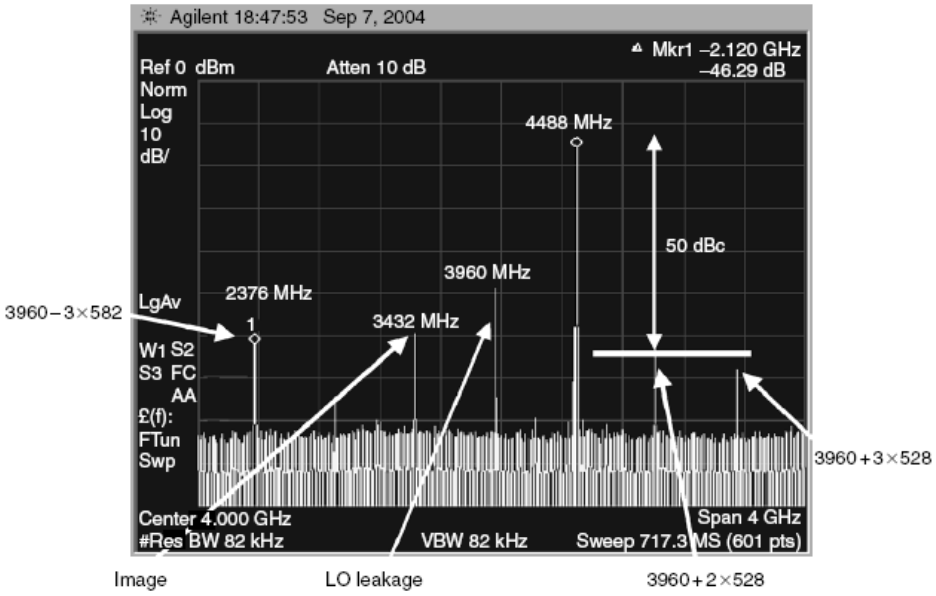


Figure 3.3: Typical SSB approach spectrum (from [40]).

3.3.3 Single PLL and SSB Mixers

Another approach is to use a single PLL to generate both required center and offset frequencies [42-45]. Generally, the PLL operates at a high frequency and provides quadrature phases by means of a quadrature VCO or a divide by-2 circuit. The offset

frequencies are tapped from dividers in the feedback path of the PLL. Depending on the number of bands they can cover, 2 or 3 SSB mixers have been used to add or subtract the offset frequencies to the center frequencies. Fig. 3.4 shows the implementation in [44] as an example. High frequency multiplexers and power hungry buffers must be used in these structures. In addition, by using 2 or 3 SSB mixers, more intermediate frequency components would be created which may cause unwanted sidebands at the output. This might necessitate the use of additional inductors to obtain more side-band suppression at the output of SSB mixers and calibration circuits to minimize the quadrature mismatch.

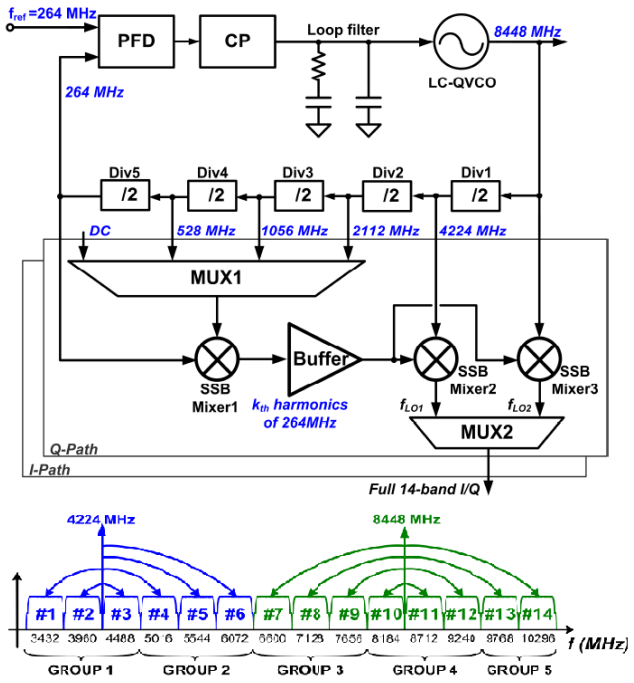


Figure 3.4: Architecture in [44].

3.3.4 Single PLL, Direct Digital Synthesizer and SSB Mixer

A synthesizer for the mandatory band using a direct digital synthesizer (DDS) is demonstrated in [46]. The center frequency is generated by means of a PLL locked to an

external reference frequency. The DDS generates the low frequencies for addition or subtraction. Inherently, the harmonics of these signals are much lower than if they had been generated by divider chains, SSB mixers, or both. A high frequency signal is used to clock the read only memory (ROM) lookup tables and current-steering DACs. The sinusoidal *I*/*Q* waveforms are stored in the ROM tables. A SSB mixer is needed to mix the center frequency signal with the output signal from the DDS. Digital circuits (ROM, DAC) operating at such frequencies consume exorbitant amount of power. This is evident from the high power consumption reported in [46]. Here the main problem is the implementation of high-frequency DDS.

3.3.5 DLL Based

In [47], a DLL-based frequency synthesizer is proposed for UWB applications. DLLs are first order systems and their bandwidth can be increased without sacrificing stability. By choosing a very wide bandwidth, settling time can be made extremely small. The architecture is based on a static 528 MHz PLL and a multiplying DLL. Frequency switching is accomplished by changing the multiplication ratio. The primary disadvantage in a conventional DLL structure is the behavior at the switching instance. Any glitches should be avoided to reduce lock time. The proposed architecture uses separate PFD-CP for each switching combination which increases the power consumption. Furthermore, due to the mismatch between delay cells in the voltage controlled delay line, this approach suffers from poor spectral purity (spurious tones are as high as -35 dBc).

3.3.6 ILO Based

Various UWB LO concepts have already been discussed, but none of them seems to give clear advantages over the other. In section 3.1, we show that a sub-harmonic injection locked oscillator acts like an integer-*N* PLL with very low power consumption. This approach has been used in [33, 34] to realize a UWB synthesizer. All UWB band frequencies are at odd harmonics of 264 MHz. Thus, the oscillator can lock to the desired harmonic (13^{th}, 15^{th} or 17^{th} harmonic for the first band) by changing the natural frequency of its *LC* tank. One can also lock the oscillator at 4 times of the frequencies of band group 1 as shown in Fig. 3.5. As a consequence, only one oscillator can cover all 14 band groups. This approach has great advantages in terms of area, complexity of routing and power consumption.

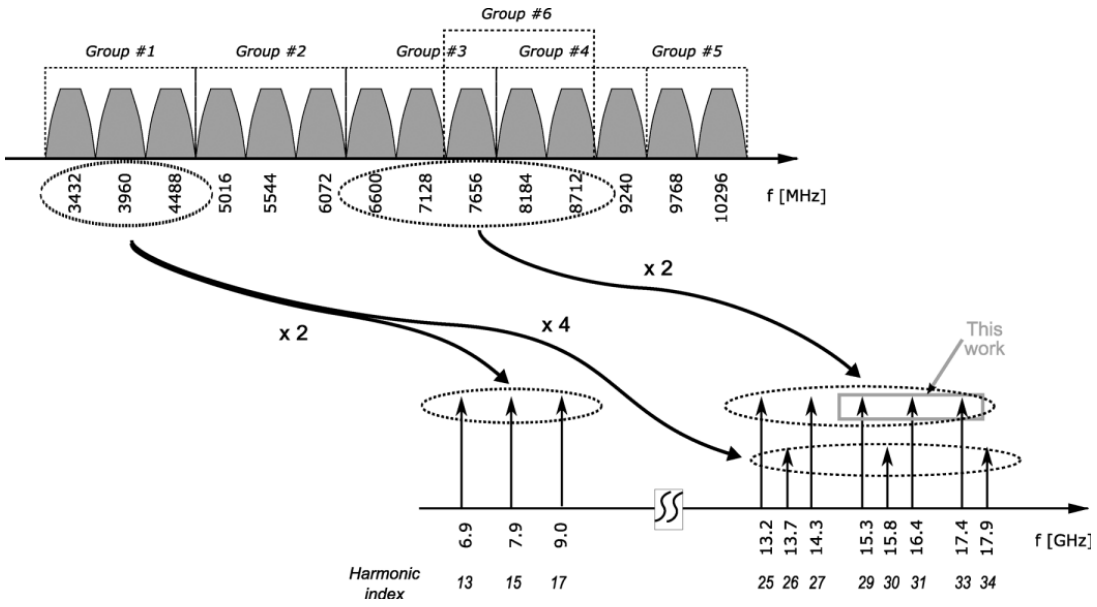


Figure 3.5: ILO-Based synthesizer frequency plan proposed in [34].

An *LC*-oscillator which is operating at twice of the center frequency of each band is followed by a divide by-2 circuit in order to generate required quadrature output [34]. Alternatively, to save more power, an injection locked quadrature oscillator is used in [33] to generate the quadrature output directly.

Although this approach shows significant power and area saving, it suffers from a very high level of spurious tone at the output (as high as -19 dBc in [34]). None of the existing ILO-based synthesizers is able to meet the spur requirement discussed in section 3.2.1. These spurious tones are mainly originated from the injection signal which is a low-duty cycle square wave. Since narrow-width pulses are relatively richer in higher frequency harmonics, such a wave form is used in order to improve the harmonic content. However, all the harmonics in that waveform have almost equal power and those which are out of locking range appear at the output with limited suppression. The remaining part of this chapter focuses on a pulse shaping technique to reduce these spurs. The proposed technique is applied to an ILO-Based UWB synthesizer as a testing vehicle and it will be shown that by using a pulse shaping technique, an ILO-based synthesizer can meet the specification described in section 3.2.1.

3.4 Spur Suppression in Injection Locked *LC* Oscillator

In this section we provide a mathematical model to predict the spurs at the output of a sub-harmonic ILO. The equation derived in this section provides a valuable insight into the design of sub-harmonic ILOs.

Predicting the relative level of spurious tones for a non-linear system like ILO is extremely difficult. In [34], a perturbation approach has been proposed, which leads to complicated mathematical derivations. Here, we show that a simple and intuitive approach can be employed to obtain a similar result. We adopt the ILO model from [22, 26] as shown in Fig. 3.6.

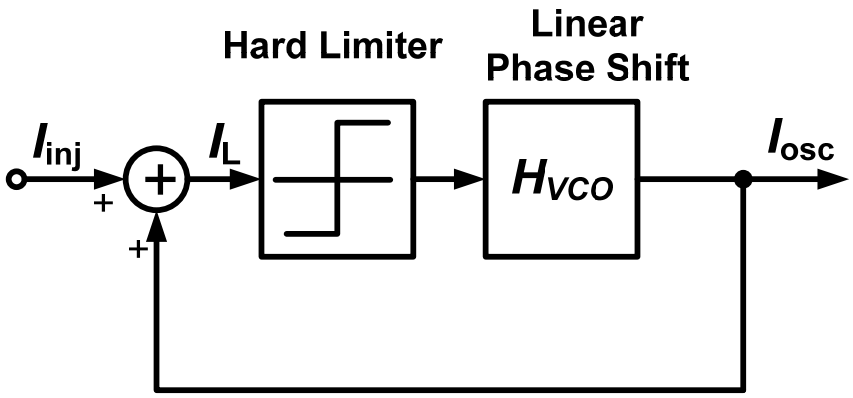


Figure 3.6: Model of oscillator under injection.

In the case of cross-coupled *LC* oscillators, non-linear block (hard-limiter) models the amplitude limiting behavior of the oscillator and the linear phase shifter is given by

$$H_{VCO}(\omega) = \frac{j\omega\left(\frac{\omega_0}{Q}\right)}{\omega_0^2 + j\omega\left(\frac{\omega_0}{Q}\right) + (j\omega)^2} \qquad (3.3)$$

We assume one of the harmonics of the reference signal falls within the locking range and locks the oscillator. We are mainly interested in estimating the relative suppression of other harmonics which are out of locking range. The positive feedback causes the system to oscillate at the free running frequency of ω_0. The input harmonic with frequency of ω_{inj} close to ω_0, experiences regeneration around the oscillation loop and amplifies with very high gain (the closed loop gain of the system is very big when

$\omega_{inj} \approx \omega_0$). The locking happens when the system amplifies this harmonic to a level close to the free running oscillation amplitude [16, 48] and therefore the output will be limited to

$$\left|I_{\text{out},\,\omega_{\text{inj}}}\right| = \left|I_{osc}\right|. \qquad (3.4)$$

Other harmonics at frequency $\omega_{inj} + \omega_m$ experience the closed loop gain as well and thus

$$\left|I_{out,\omega_{inj}+\omega_m}\right| = \left|I_{spur}\right| = \left|\frac{H_{VCO}(\omega)}{1-H_{VCO}(\omega)}\right|_{\omega=\omega_{inj}+\omega_m} \cdot \left|I_{inj,\omega_{inj}+\omega_m}\right|$$

$$\approx \left|\frac{\omega\omega_0}{Q(\omega^2-\omega_0^2)}\right|_{\omega=\omega_{inj}+\omega_m} \cdot \left|I_{inj}\right|. \qquad (3.5)$$

In (3.5), we have assumed $\left|I_{inj,\omega_{inj}+\omega_m}\right| \approx \left|I_{inj,\omega_{inj}}\right| \approx \left|I_{inj}\right|$, which is usually the case for sub-harmonic ILOs where higher frequency harmonics are employed as the desired injection signal. Also, since the gain is smaller in this case, the amplitude is much smaller than free running oscillation amplitude and thus the amplitude limiting does not occur. From (3.4) and (3.5), relative level of spurious tones at the output will be

$$\frac{\left|I_{\text{spur}}\right|}{\left|I_{out,\omega_{inj}}\right|} = \frac{(\omega_{inj}+\omega_m)\omega_0}{Q(\omega_{inj}+\omega_m-\omega_0)(\omega_{inj}+\omega_m+\omega_0)} \cdot \frac{\left|I_{inj}\right|}{\left|I_{osc}\right|} \qquad (3.6)$$

Under normal sub-harmonic ILO operation, $\omega_{inj} \approx \omega_0$ and $\omega_m << \omega_{inj}$, (3.6) is simplified to

$$\frac{\left|I_{\text{spur}}\right|}{\left|I_{desired}\right|} \approx \frac{\omega_0}{2Q\omega_m} \cdot \frac{\left|I_{inj}\right|}{\left|I_{osc}\right|} = \frac{\omega_L}{\omega_m} \qquad (3.7)$$

which is the same result obtained in [7] using the perturbation approach.

Equation (3.7) along with (2.33) provides valuable insights into the design of sub-harmonic ILO synthesizer. Increasing the locking range decreases the locking time and spurs suppression at the output. In applications where hopping time is not critical, one can decrease the locking range to reduce the spurs at the output. However, in practice, reduced locking range increases the danger of losing lock as the VCO's free running frequency might deviate significantly from the intended reference harmonic due to process, voltage and temperature (PVT) variations. For fast switching applications, the locking range is pre-determined by switching time requirement and spur suppression would be limited. To address this trade-off, we study the harmonic content of different pulse shapes in detail and propose a pulse shaping technique to relax the above-mentioned trade-off and achieve higher spur suppression.

3.5 Harmonic Reduction Theory

To explain the theory behind our pulse shaping technique, we focus on generation of the first band group of UWB specification (Fig. 3.1) which corresponds to the 13th, 15th and 17th harmonic of a 264 MHz reference signal. Nevertheless, the analysis provided here is generic and can be extended to other harmonics of interest or sub-harmonic ILOs.

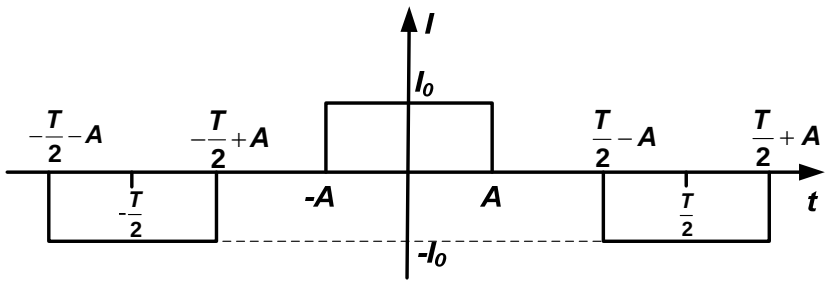


Figure 3.7: Differential (symmetric) square wave with pulse width of 2A.

Traditionally differential circuits have been used to suppress even harmonics in circuits, which is adopted in our design as well. Fig. 3.7 shows a differential (symmetric) square wave with pulse width of $2A$, amplitude of I_0 and period of $T=2\pi/\omega_0$. The spectrum of this pulse is a sinc function and its characteristics vary significantly with pulse width. The harmonic content of this pulse train can be obtained through Fourier series expansion:

$$I(t) = \sum_{n=1}^{\infty} a_n \cos(n\omega_0 t) + b_n \sin(n\omega_0 t) \qquad (3.8)$$

where

$$a_n = \begin{cases} \frac{4I_0}{n\pi}\sin(n\omega_0 A) & for\ odd\ n \\ 0 & for\ even\ n \end{cases} \qquad (3.9)$$

and $b_n=0$ for all n. For pulse width of $2A=T/2$,

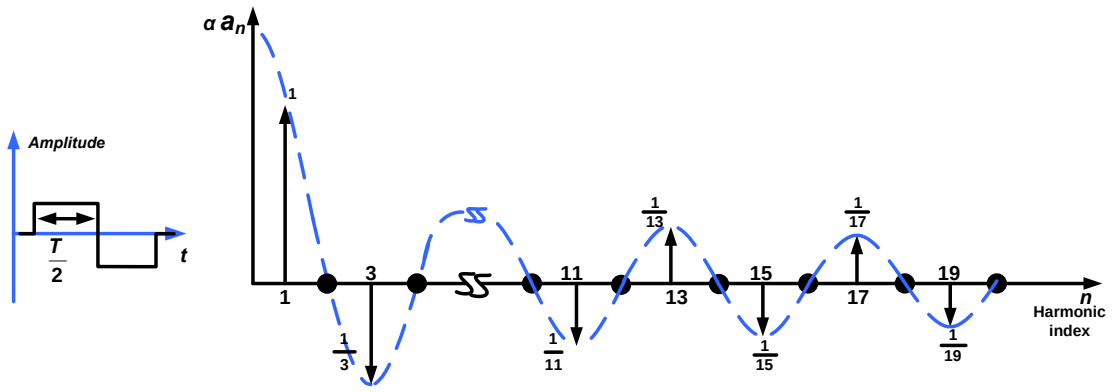
$$a_n\big|_{A=\frac{T}{4}} = \frac{4I_0}{n\pi}\sin(\frac{n\pi}{2}) \qquad (3.10)$$

where amplitude of the n^{th} harmonic is inversely proportional to n. The resulting Fourier coefficients exhibit positive sign for $n=4k+1$ and negative sign for $n=4k-1$(k=1, 2, 3,…)[Fig. 3.8(a)]. If we reduce the pulse width by 15, i.e. $2A=T/(2\times15)$,

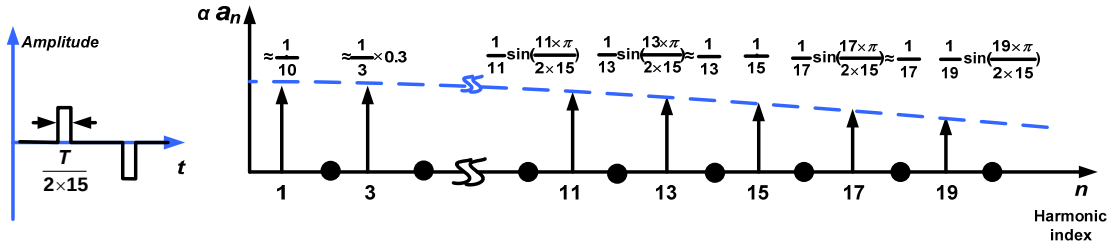
$$a_n\big|_{A=\frac{T}{4\times15}} = \frac{4I_0}{n\pi}\sin(\frac{n\pi}{2}.\frac{1}{15}). \qquad (3.11)$$

Amplitude of the lower order harmonics is reduced while amplitude of the harmonics of interest (13th, 15th, and 17th) remains relatively unchanged as shown in Fig. 3.8(b). From (3.10) and (3.11), amplitude of the 15th harmonic ($n=15$) is equal for both pulses but with opposite sign, i.e. $a_{15}\big|_{A=\frac{T}{4\times15}} = -a_{15}\big|_{A=\frac{T}{4}} = \frac{4I_0}{15\pi}$. In addition, amplitude of the adjacent

harmonics, a_{13} and a_{17}, for the narrow pulse ($2A=T/(2\times15)$) closely approximates the amplitude of the corresponding harmonics for the wider pulse with same polarity, i.e. $a_{13}\big|_{A=\frac{T}{4\times15}} \approx a_{13}\big|_{A=\frac{T}{4}} = \frac{4I_0}{13\pi}$, and $a_{17}\big|_{A=\frac{T}{4\times15}} \approx a_{17}\big|_{A=\frac{T}{4}} = \frac{4I_0}{17\pi}$. This approximation is valid due to the fact that the value of the sine function does not change considerably when its argument deviates slightly from $\pi/2$.



(a)



(b)

Figure 3.8: Time domain and spectrum of a differential pulse with (a) width of $T/2$. (b) width of $T/(2\times15)$.

Based on the above observations on amplitude and polarity of the harmonics for both pulses, one can create the injection signal with selective harmonic content through simple algebraic combination of the above mentioned pulses. Fig. 3.9(a) shows the

resulting waveform and its corresponding Fourier transform in the band of interest obtained by adding the two pulses together. As illustrated, the 13th and 17th harmonics are enhanced while the 11th, 15th and 19th harmonics are suppressed by at least 26 dB. This pulse will be used for injection to the oscillator to generate the center frequency of the first and third band of UWB system (13th and 17th harmonics).

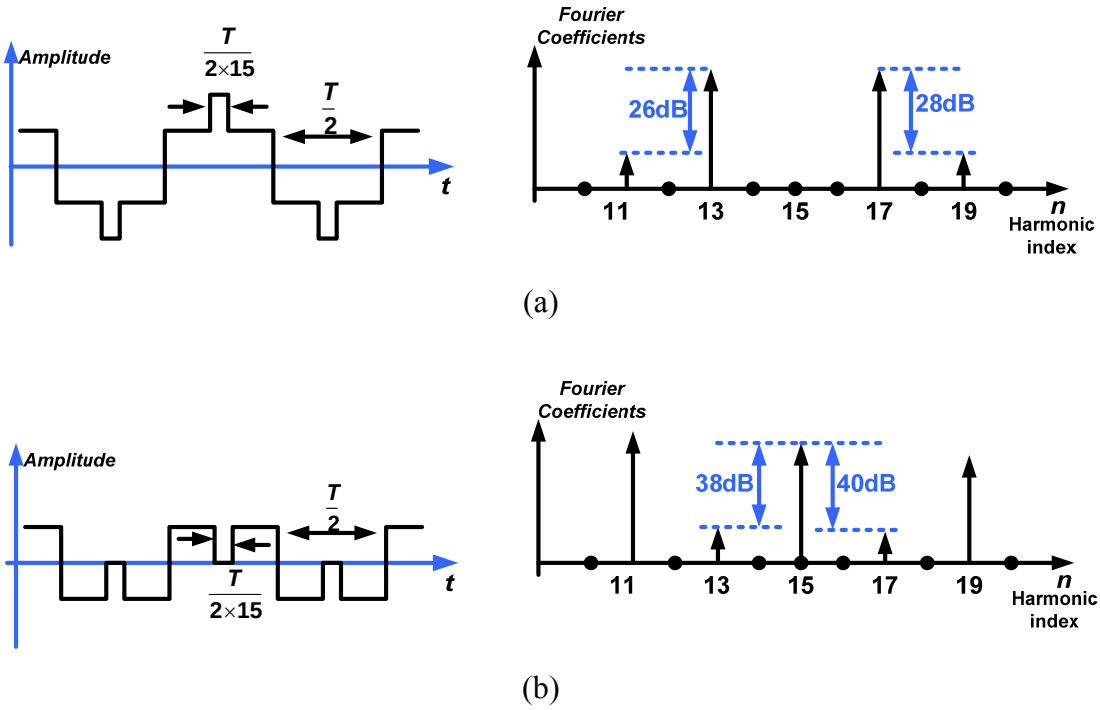


Figure 3.9: Effective waveforms and their spectrums for generation of (a) 13th and 17th harmonic. (b) 15th harmonic.

Fig. 3.9(b) shows the alternative waveform and its spectrum by subtracting the two pulses. In this scenario, the 11th, 15th and 19th harmonics are enhanced while the 13th and 17th harmonics are suppressed by 38 and 40 dB respectively. We will use this pulse as an injection signal to the oscillator to generate the center frequency of the second band (15th harmonic). As illustrated, this pulse shaping suppresses the unwanted harmonics in

the pulse generator before injection into the oscillator and therefore abates the trade-off between locking time and spectral purity.

The relative level of spurious tones can be obtained using (3.10) and (3.11). For example, relative suppression between the unwanted 13th harmonic and the desired 15th harmonic for the waveform in Fig. 3.9(b) is given by

$$HR_{15-13} = 20\log\left|\frac{|a_{13}|_{A=\frac{T}{4}} - |a_{13}|_{A=\frac{T}{4\times 15}}}{|a_{15}|_{A=\frac{T}{4}} + |a_{15}|_{A=\frac{T}{4\times 15}}}\right| = -38\text{dB}. \qquad (3.12)$$

Note that this amount of suppression is achieved only by shaping the injection signal. Additional spur suppression provided by ILO based on (3.7) will be added to this amount at the synthesizer output. It should also be pointed out that this technique can be easily extended to higher UWB band groups using pulses with different width (*2A*).

3.6 Circuit Implementation

The block level architecture for our test chip is shown in Fig. 3.10. A digitally controlled oscillator (DCO) is operating at twice the desired frequencies to avoid frequency pulling by power amplifier of the transmitter. A spur suppressing pulse generator (SSPG) based on earlier discussion provides the injection signal to the oscillator. The oscillator is designed to cover the first band group of the UWB specification. The corresponding injection signal frequencies provided by SSPG are the 13th, 15th and 17th harmonics of a 528 MHz reference signal. DCO is injection-locked to the required harmonic by tuning its free running frequency close to that harmonic. The

frequency and band-switching control words to DCO and SSPG are obtained from serial peripheral interface. Upon powering up, control words for each band are searched and stored such that the free running frequency for each band remains close to the desired reference harmonic to compensate for PVT variation. We did not include any frequency calibration circuit in this implementation. However, a calibration technique similar to [49] and [50] can be easily applied if needed. A multiplexer (MUX) is used to switch between two different DCO control words for band hopping. The select input of the MUX is buffered on-chip to ensure fast rise/fall time and minimize its impact on frequency hop time. The implementation of various building blocks will be presented next.

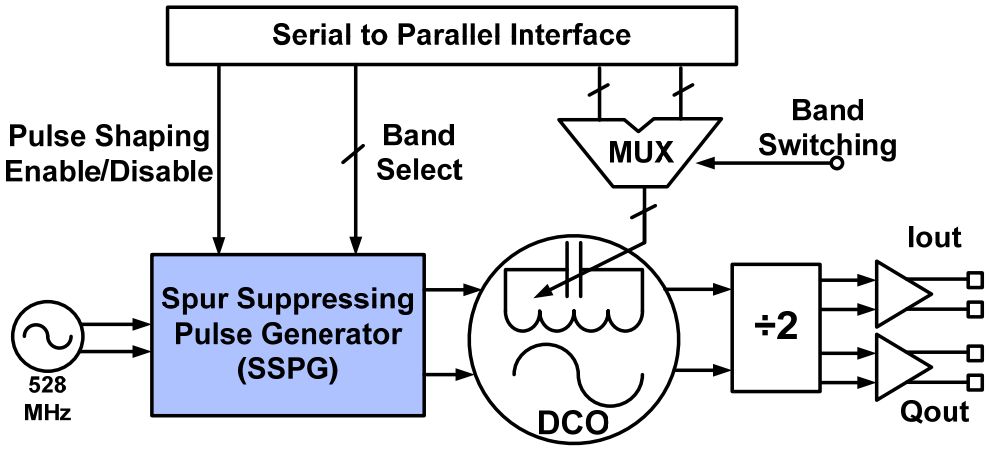


Figure 3.10: Block diagram of the test chip.

3.6.1 Spur Suppressing Pulse Generator

To generate the combined waveforms shown in Fig. 3.9, the main challenge lies in aligning the center of both pulses. Fig. 3.11 shows the circuit that achieves this task. An AND operation is used between the input reference and its delayed replica by

$2\times D$ (X) to generate the narrow pulse (Z) with $2A = \frac{T}{2} - 2D = \frac{T}{2\times 15}$. The pulse width can be adjusted by changing the delay (D). Delayed replica of the input reference with $1\times D$ delay (Y) is employed as the wider pulse with $2A = T/2$. As illustrated in the timing diagram, alignment of the two pulses can be achieved if the delay cells match each other. To maintain good matching of the delay cells, a dummy delay cell is added to provide identical loading for each cell. In addition, A_2 is used to replicate the delay associated with A_1 and avoid any systematic delay mismatch in the signal paths.

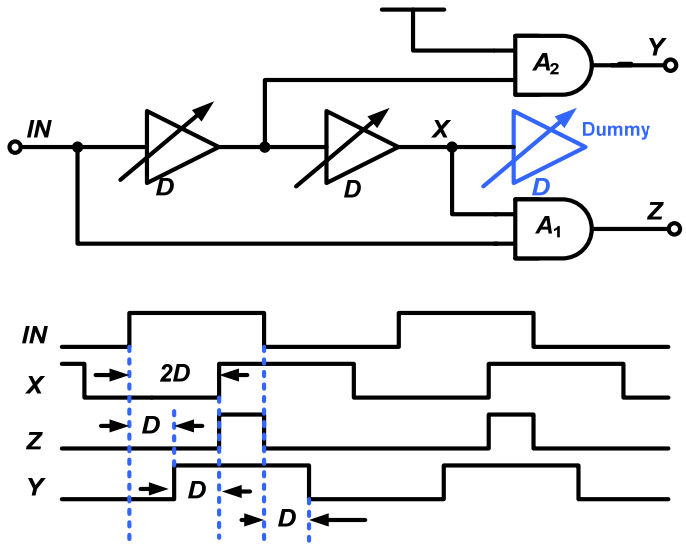
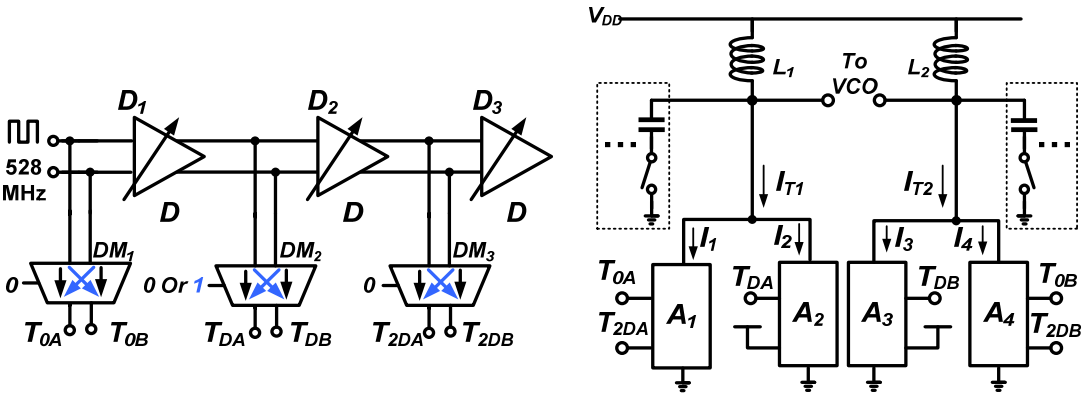


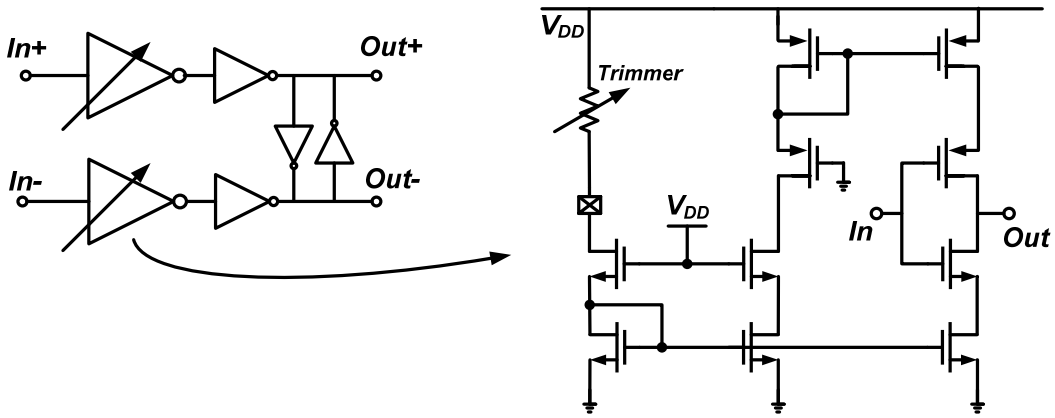
Figure 3.11: Conceptual diagram of the timing generator.

Final implementation is shown in Fig. 3.12(a). D_1-D_3 form the delay line. Pseudo-differential operation is chosen to suppress even harmonics without consuming any static power. Differential implementation also improves common-mode noise rejection. Current-starved inverters are used to implement the variable delay cells as shown in Fig. 3.12(b). In this implementation, the delay is varied through an off-chip trimmer as illustrated in Fig. 3.12(b). Cross-coupled inverters are utilized to maintain 50% duty

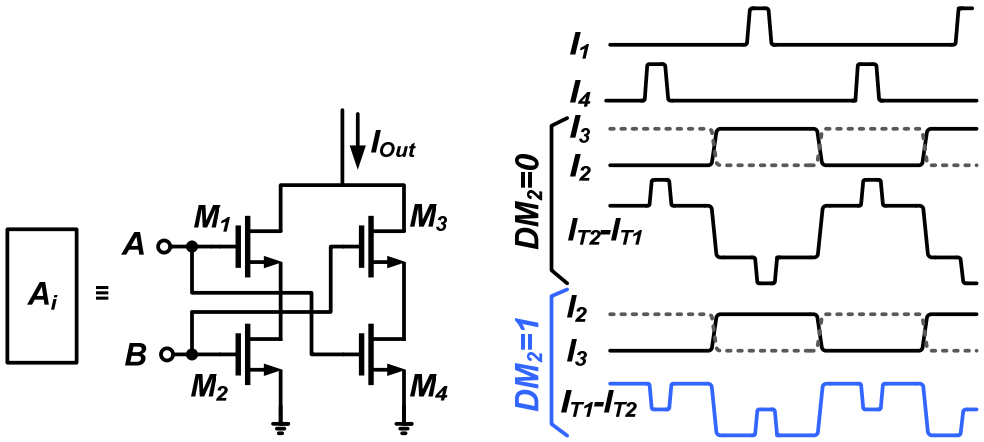
cycle for the signals. This duty cycle correction is critical for even harmonics suppression of the synthesized output, which will be discussed later.



(a)



(b)



(c) (d)

Figure 3.12: (a) Schematic of SSPG. (b) Pseudo-differential delay cell. (c) Symmetric current-mode AND. (d) Timing diagram of the operation of SSPG in different bands.

In this work, we size the cross-coupled inverters about one third of the inverters in the delay cell. According to Monte-Carlo simulation, duty cycle error can be more than 3.3% without cross-coupled inverters and is improved to less than 0.67% with cross-coupled inverters.

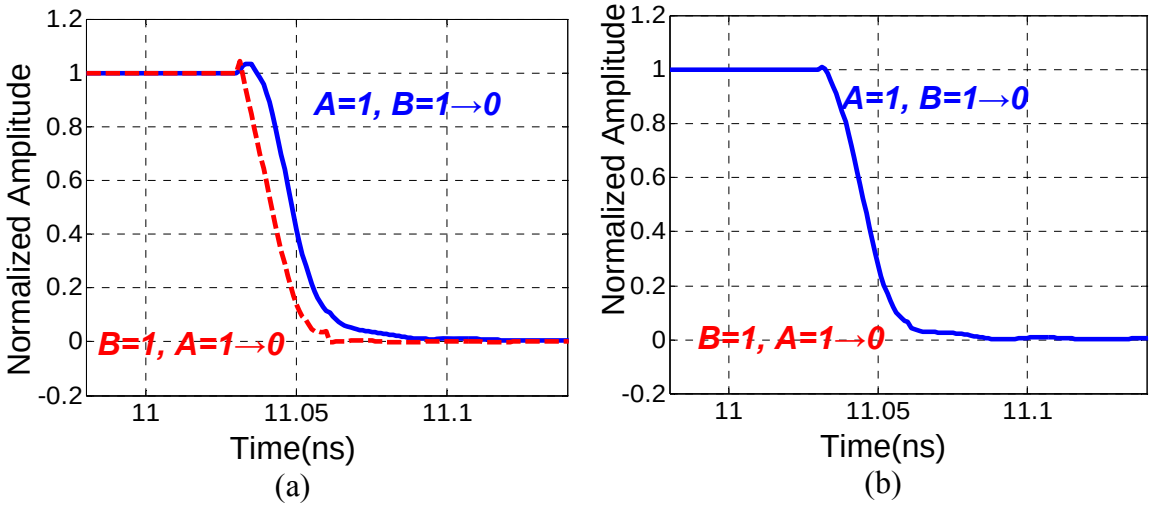


Figure 3.13: Simulated delay of an AND gate (a) without (b) with proposed symmetric PDN.

Our simulations in 0.13 μm CMOS show that conventional CMOS static AND fails to generate a narrow pulse with width of $2A=T/(2\times15)\approx63$ps reliably across all process corners and temperatures. To circumvent this problem, a symmetric current-mode AND shown in Fig. 3.12(c) is proposed, which offers several advantages. Firstly, static CMOS AND relies on voltage operation and charging/discharging of the output capacitance limit the maximum achievable operation frequency. In contrast, current-mode AND only involves output current switching and could operate faster. In addition, eliminating the PMOS pull up transistors reduces the fan-out of the previous stage and allows faster operation. Secondly, in the conventional pull down network (PDN) (only M_1

and M_2), the delay of the gate depends upon the data input pattern [51]. This input pattern dependency changes the width of the pulses in different signal paths and causes misalignment between the pulses. Fig. 3.13 shows the simulated transient behavior of the gate for different input patterns without and with symmetric PDN. As shown, undesired delay difference is completely eliminated in the latter case. Finally, output current from different AND gates can sum together into inductive loads as shown in Fig. 3.12(a). This summation is required to shape the injection signal (I_{T1}–I_{T2}) and suppress the unwanted harmonics. Besides, the required subtraction of the currents for pulse shaping (Fig. 3.9(b)) can be easily obtained by swapping the input of A_2 and A_3 through DM_2. DM_1 and DM_3 are used to replicate the delay associated with DM_2 into other signal paths and avoid systematic delay mismatch. The inductive load in the gate uses the same inductor and switched capacitor as the DCO and the same frequency code word is used to control both capacitor banks. Fig. 3.12(d) shows the timing diagram and shape of differential output current (I_{T1}–I_{T2}) in different modes of operation.

3.6.2 Digitally Controlled Oscillator

Fig. 3.14 shows the *LC* oscillator and the method of injection. Here, coupling pair M_3–M_4 receives differential output from SSPG at its gates and injects the corresponding current into the *LC* tank. The locking range mainly depends on the ratio of I_{inj}/I_{osc} which is process and temperature insensitive. A double turn 800 pH differential inductor and 6-bits of binary weighted switched-capacitor bank are employed to realize the *LC* tank. The two least significant bits are implemented by means of MOM capacitors while the four most significant bits are made of MIM capacitors. The output after divide by two is

measured to tune from 3.180 to 4.720 GHz with frequency resolution of smaller than 85 MHz at the higher end of the tuning range. The simulated tuning range was from 3.02 to 5 GHz. The lock range of the DCO is also measured to be about 100 MHz.

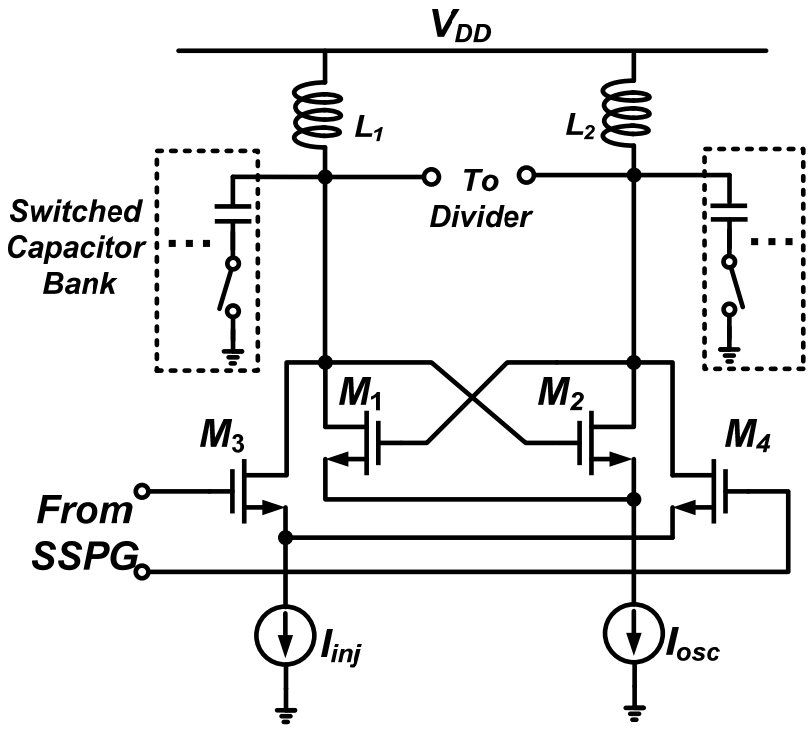


Figure 3.14: Schematic of the *LC* DCO and injection pair.

3.6.3 Frequency Divider

Fig. 3.15 reveals the divider design which is a static topology with class AB CML latches [52]. Since the tail current is removed, M_9-M_{12} can be narrower, presenting a smaller capacitance to the DCO. Besides, drain currents of M_9-M_{12} are not limited by a tail current. Simulation shows that at the peak of the clock swing, these transistors draw an instantaneous larger current which boost the operation frequency.

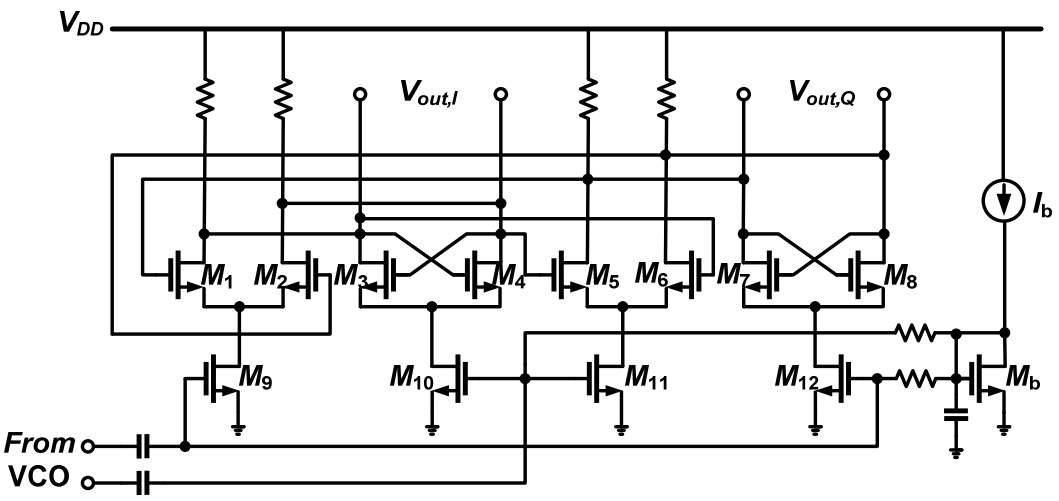


Figure 3.15: Class AB CML divide-by-two.

3.7 Effect of Non-Idealities

There are four types of error that affect the spur suppression as shown in Fig. 3.16. The first one is the pulse position error, which is due to the misalignment of two pulses. The main contributor to this error is the mismatch between the delay cells. The second type of error is the deviation of the pulse width from $T/(2\times 15)$ which is introduced by the variation of delays due to PVT. The third type of error is the pulse width imbalance. Cross-coupled inverters are employed to reduce this effect. However, there might still be some residual error which we will investigate here. The last type of error is the amplitude imbalance, which is introduced by mismatch between currents of the AND gates. The first two types of errors degrade the effectiveness of spur suppression while the last two contribute to even harmonics generation. In the following subsections, these effects will be analyzed. It should be noted that the analysis is performed on the injection signal rather than the ILO synthesized output.

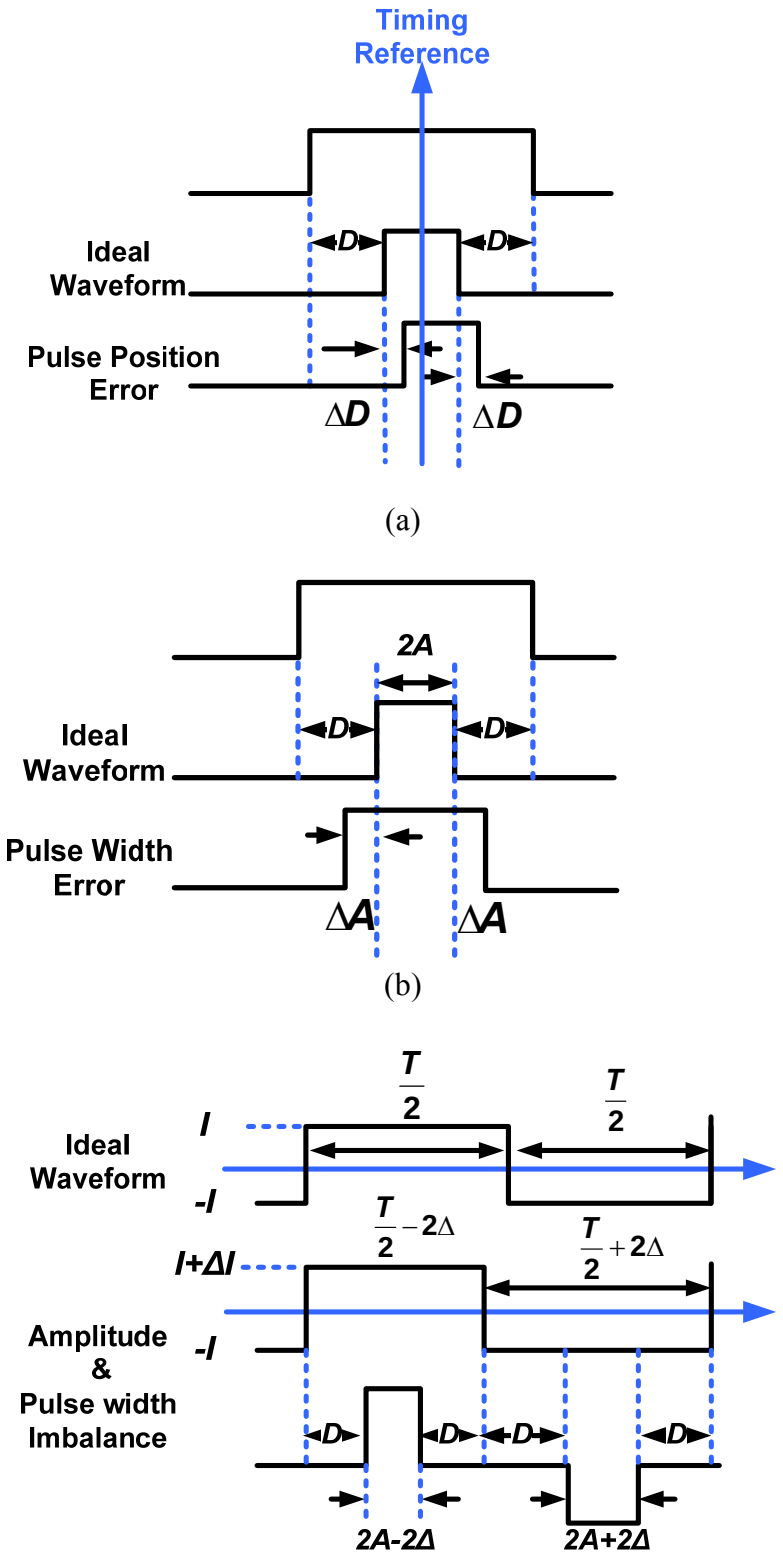


Figure 3.16: (a) Pulse position error. (b) Pulse width error. (c) Amplitude and pulse-width imbalance.

3.7.1 Pulse Position Error

We assume that we have a wide pulse (f_W) with pulse width of $2A=T/2$ and a narrow pulse (f_N) with pulse width of $2A=T/(2\times15)$. To simplify the derivations, we further assume that f_W is symmetric around our timing reference as shown in Fig. 3.16(a). The spectral content can be obtained through Fourier analysis:

$$f_W(t) = \sum_{n=1}^{\infty} a_{n,w} \cos(n\omega_0 t) \qquad (3.13)$$

where

$$a_{n,W} = \begin{cases} \dfrac{4I_0}{n\pi}\sin(\dfrac{n\pi}{2}) & odd \quad n \\ 0 & even \quad n \end{cases} \qquad (3.14)$$

Assuming ΔD mismatch between delay cells with nominal delay $D=T/4-A$ and $A=T/(4\times15)$, the Fourier expansion for f_N can be simplified to

$$f_N(t) = \sum_{n=1}^{\infty} a_{n,N} \cos(n\omega_0 t) + b_{n,N} \sin(n\omega_0 t) \qquad (3.15)$$

where

$$a_{n,N} = \begin{cases} \dfrac{4I_0}{n\pi}\sin(\dfrac{n\pi A}{T})\cos(\dfrac{2n\pi\Delta D}{T}) & odd \quad n \\ 0 & even \quad n \end{cases} \qquad (3.16)$$

and

$$b_{n,N} = \begin{cases} \dfrac{4I_0}{n\pi}\sin(\dfrac{n\pi A}{T})\sin(\dfrac{2n\pi\Delta D}{T}) & odd \quad n \\ 0 & even \quad n \end{cases} \qquad (3.17)$$

Combination of the pulses for generation of the 13th and 17th harmonic (Fig. 3.9(a)) is given by

$$f_{ADD}(t) = f_N + f_W = \sum_{n=1}^{\infty} a_{n,ADD}\cos(n\omega_0 t) + b_{n,ADD}\sin(n\omega_0 t) \qquad (3.18)$$

where $a_{n,ADD} = a_{n,N} + a_{n,W}$ and $b_{n,ADD} = b_{n,N}$. Based on (3.18), the relative suppression between n^{th} and m^{th} harmonic for $\alpha = \Delta D/D$(%) mismatch between delay cells is given by

$$HR_{m-n} = 20\log\left.\frac{\sqrt{a_{n,ADD}^2 + b_{n,ADD}^2}}{\sqrt{a_{m,ADD}^2 + b_{m,ADD}^2}}\right|_{\frac{\Delta D}{D}=\alpha} \qquad (3.19)$$

Suppression of the 11th and 15th harmonic relative to the 13th harmonic based on the above formula is shown in Fig. 3.17(a). As illustrated, the delay mismatch can be as high as 1% while attaining harmonic suppression greater than 20 dB. The results for suppression of the 15th and 19th harmonic relative to the 17th harmonic are very similar to Fig. 3.17(a). Therefore from now on, we only plot the harmonic suppression relative to 13th harmonic for the pulse shape of Fig. 3.9(a).

Similarly, combination of the pulses for generation of the 15th harmonic (Fig. 3.9(b)) is given by

$$f_{SUB}(t) = f_N - f_W = \sum_{n=1}^{\infty} a_{n,SUB}\cos(n\omega_0 t) + b_{n,SUB}\sin(n\omega_0 t) \qquad (3.20)$$

where $a_{n,SUB} = a_{n,N} - a_{n,W}$ and $b_{n,SUB} = b_{n,N}$. Based on (3.20), the relative suppression between n^{th} and m^{th} harmonic for α(%) mismatch between delay cells is given by

$$HR_{m-n} = 20\log\left.\frac{\sqrt{a_{n,SUB}^2 + b_{n,SUB}^2}}{\sqrt{a_{m,SUB}^2 + b_{m,SUB}^2}}\right|_{\frac{\Delta D}{D}=\alpha} \qquad (3.21)$$

Suppression of the 13th and 17th harmonic relative to the 15th harmonic based on (3.21) is depicted in Fig. 3.17(b). As illustrated, the delay mismatch can be as high as 1% while attaining harmonic suppression better than 19 dB.

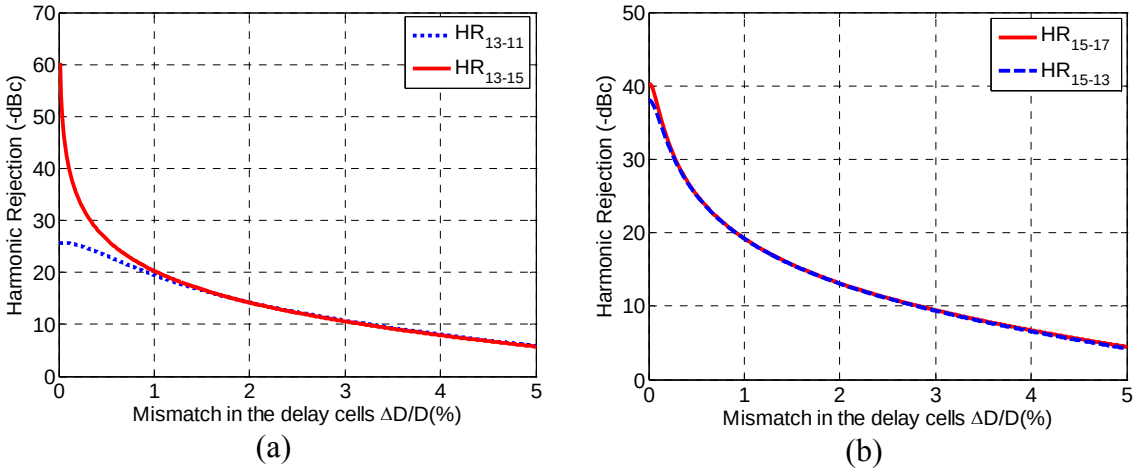


Figure 3.17: Effect of delay mismatch on harmonic reduction (a) for 13th harmonic. (b) for 15th harmonic.

3.7.2 Pulse Width Error

Using (3.13) to (3.21), by modifying A, we can investigate the effect of pulse width on the harmonic suppression. Fig. 3.18 shows the suppression of harmonics in different bands versus pulse width error. As can be seen, a pulse width error as big as 15% can be tolerated to achieve spur reduction greater than 20 dB. It is also possible to change the pulse width by setting $2A = T/(2\times 13)$ or $2A = T/(2\times 17)$ to achieve the best performance for each band. One can use a replica delay line or reconfigure the delay line into a ring oscillator, and use a digital calibration technique similar to [53] on the delay line. Such a calibration has smaller power and area overhead compared to a delay locked loop. In this design, we did not implement the calibration. As we did not provide

additional test point to measure the exact pulse width error, this effect will be studied through delay variation and sensitivity investigation discussed in section 3.8.

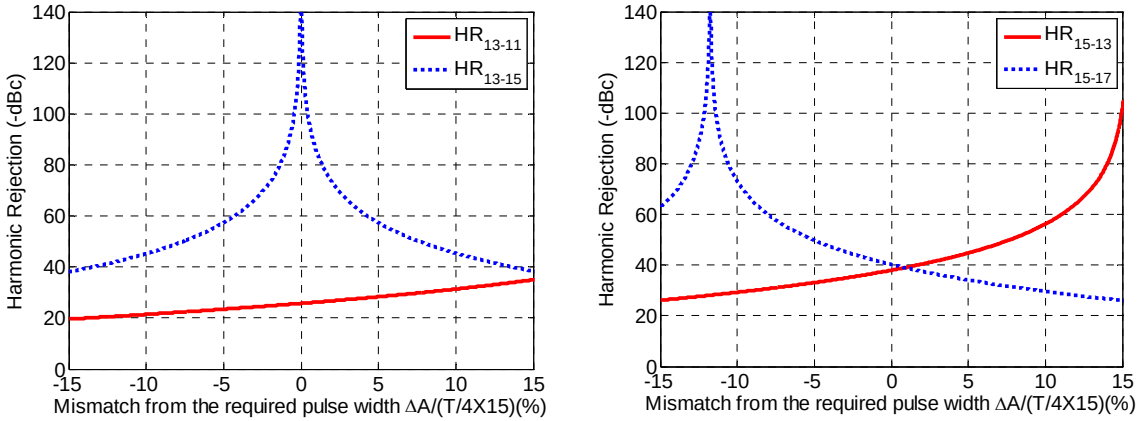


Figure 3.18: Effect of narrow pulse width on harmonic reduction (a) for 13th harmonic. (b) for 15th harmonic.

3.7.3 Amplitude and Pulse Width Imbalance Error

Assuming an amplitude error of ΔI and pulse width error of 2Δ, an imbalanced signal shown in Fig. 3.16(c) is $I_{\mathrm{Im}balanced}(t) = \sum_{n=1}^{\infty} a_n \cos(n\omega_0 t) + b_n \sin(n\omega_0 t)$ where,

$$a_n = \begin{cases} \frac{2I_0}{n\pi}(1+\frac{\Delta I}{I_0})\sin(\frac{2n\pi}{T}(A-\Delta)) + \frac{2I_0}{n\pi}\sin(\frac{2n\pi}{T}(A+\Delta)) & for\ odd\quad n \\ \frac{2I_0}{n\pi}(1+\frac{\Delta I}{I_0})\sin(\frac{2n\pi}{T}(A-\Delta)) - \frac{2I_0}{n\pi}\sin(\frac{2n\pi}{T}(A+\Delta)) & for\ even\quad n \end{cases} \qquad (3.22)$$

and b_n=0 for all n.

As shown in Fig. 3.16(c), the pulse imbalance error originates from the duty cycle error of the wide pulse (f_W). Here we define the imbalanced signals by

$$f_{W,imb} = I_{\mathrm{Im}\,balanced}\Big|_{A=\frac{T}{4}} \qquad (3.23)$$

and

$$f_{N,imb} = I_{\mathrm{Im}\,balanced}\Big|_{A=\frac{T}{4\times 15}} \qquad (3.24)$$

Similar analysis as section 3.7.1 can be done by using equations (3.22)-(3.24) to obtain the suppression of even harmonics relative to required harmonics. Assuming that the duty cycle error is $\varepsilon = \dfrac{0.5T - 2\Delta}{T} - \dfrac{1}{2}$, Fig. 3.19 shows the suppression of even harmonics with respect to desired harmonics for different value of amplitude and duty cycle error. As illustrated, amplitude error has negligible effect on the performance. Moreover, according to Monte-Carlo simulation, 3σ variation of duty cycle error is less than 0.67% which corresponds to even harmonic suppression greater than 24 dB.

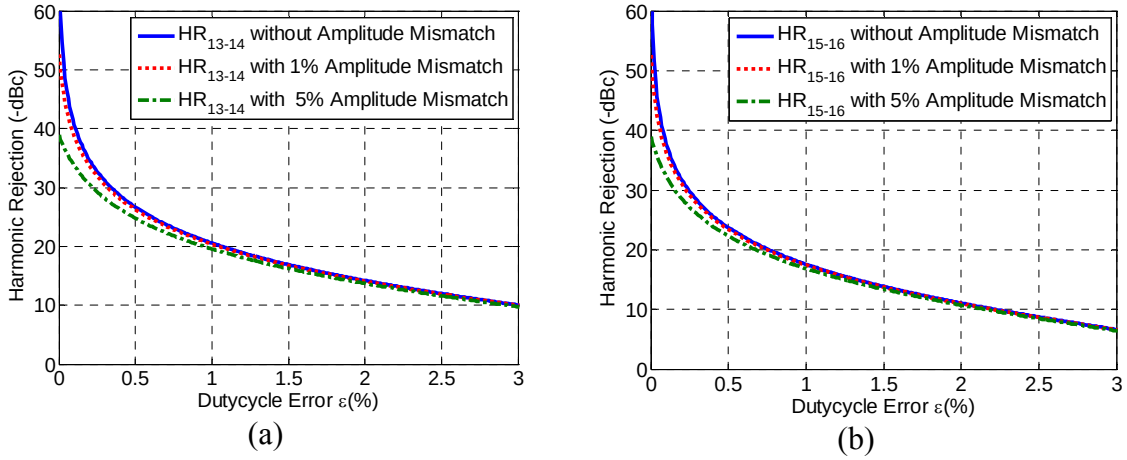


Figure 3.19: Effect of amplitude and pulse width imbalance on even harmonic rejection (a) relative to 13th harmonic. (b) relative to 15th harmonic.

3.8 Experimental Results

The test chip tailored to the first band group of WiMedia-UWB has been fabricated in standard 0.13 μm CMOS technology. Fig. 3.20 shows a micrograph of the die which occupies an active core area of 0.15 mm^2. The chip is packaged in Quad Flat No lead (QFN) and all the measurements have been performed on the packaged chips. The chip consumes a total current of 18 mA from a single 1.2-V supply. Injection-locked DCO, divider, AND gate and timing generator consumes 6.1, 3.5, 4.4 and 4 mA respectively.

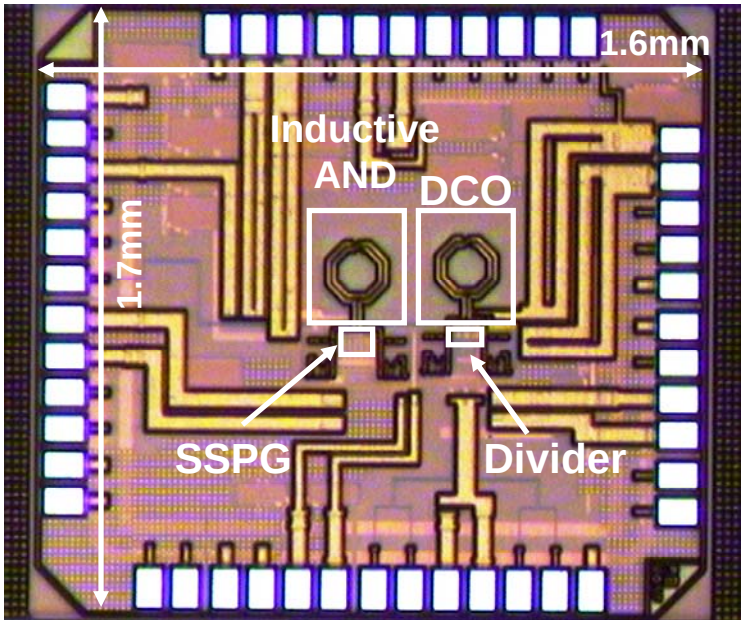
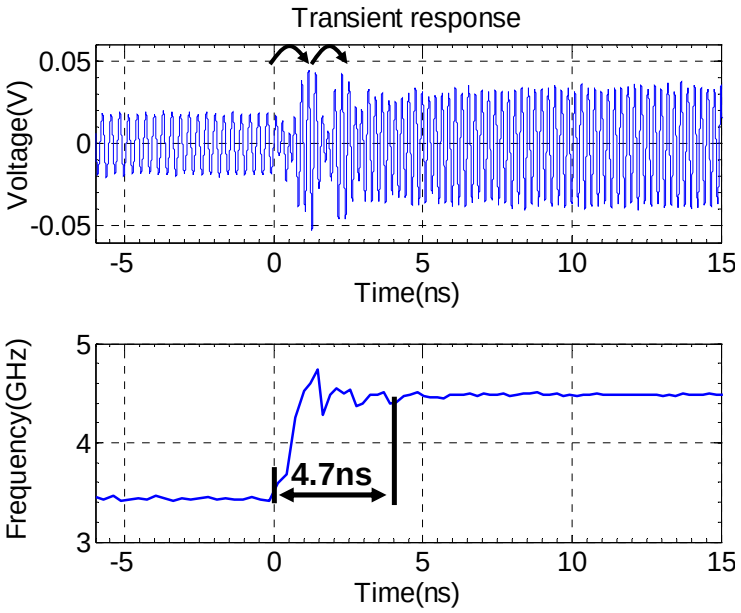


Figure 3.20: Die micrograph.

In order to measure the hopping time, the output is sampled on a 50 GS/s Tektronix DPO71254 real time oscilloscope to obtain the transient data. Instantaneous frequency can then be extracted from the zero crossings after post processing with MATLAB. Fig. 3.21(a) shows the worst case hopping time of 4.7 ns between band 1 and

band 3. The measured switching time for all combinations of band switching is shown in Fig. 3.21(b). The minimum switching time is 3.3 ns.



(a)

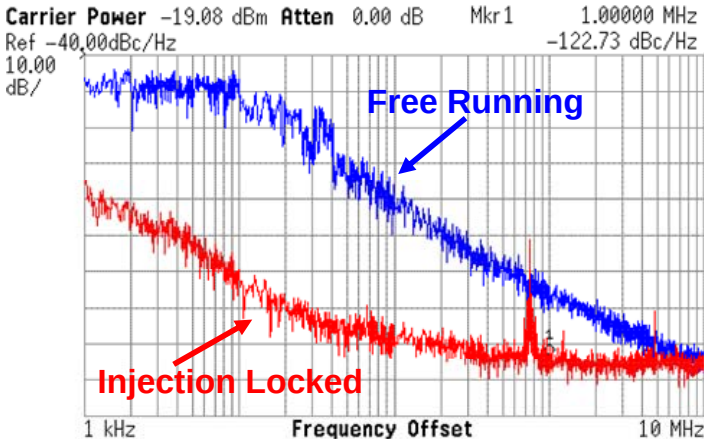
From \ To	Band 1	Band 2	Band 3
Band 1	-	4.5	4.7
Band 2	3.6	-	3.3
Band 3	4	3.6	-

(b)

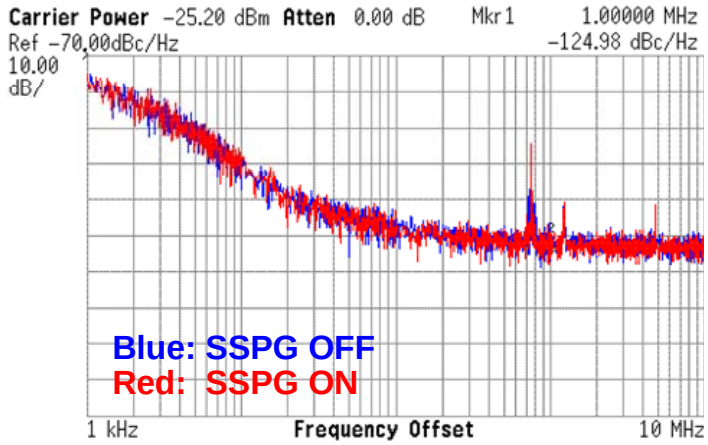
Figure 3.21: (a) Measured hopping time from Band 1 to Band 3. (b) Measured switching time for all bands (ns).

Phase noise of the synthesizer is measured on a standard Agilent E4407B spectrum analyzer while Agilent E4438C is used to provide the 528 MHz reference. Fig. 3.22(a) shows the phase noise at the third band (4488 MHz). In free running, the phase noise is -105 dBc/Hz at 1 MHz offset while under injection locking, it improves to -122 dBc/Hz at the same offset. Fig. 3.22(b) shows the phase noise measurement for the first band with SSPG on and off overlapped on each other. As can be seen, there is no

observable difference between the two. This observation shows that the pulse shaping has negligible impact on phase noise.



(a)



(b)

Figure 3.22: (a) Measured phase noise of Band 3 in free running and locked condition. (b) Measured phase noise of Band 1 with SSPG on and off.

Fig. 3.23(a)-(c) show the measured output spectrum for all bands. The spurs at 1056 MHz offset are suppressed by pulse shaping and they are all below -47 dBc. To prove the effectiveness of our proposed technique, the output with conventional injection pulse is also measured in Fig. 3.23(d) and it exhibits spur level as high as -25 dBc.

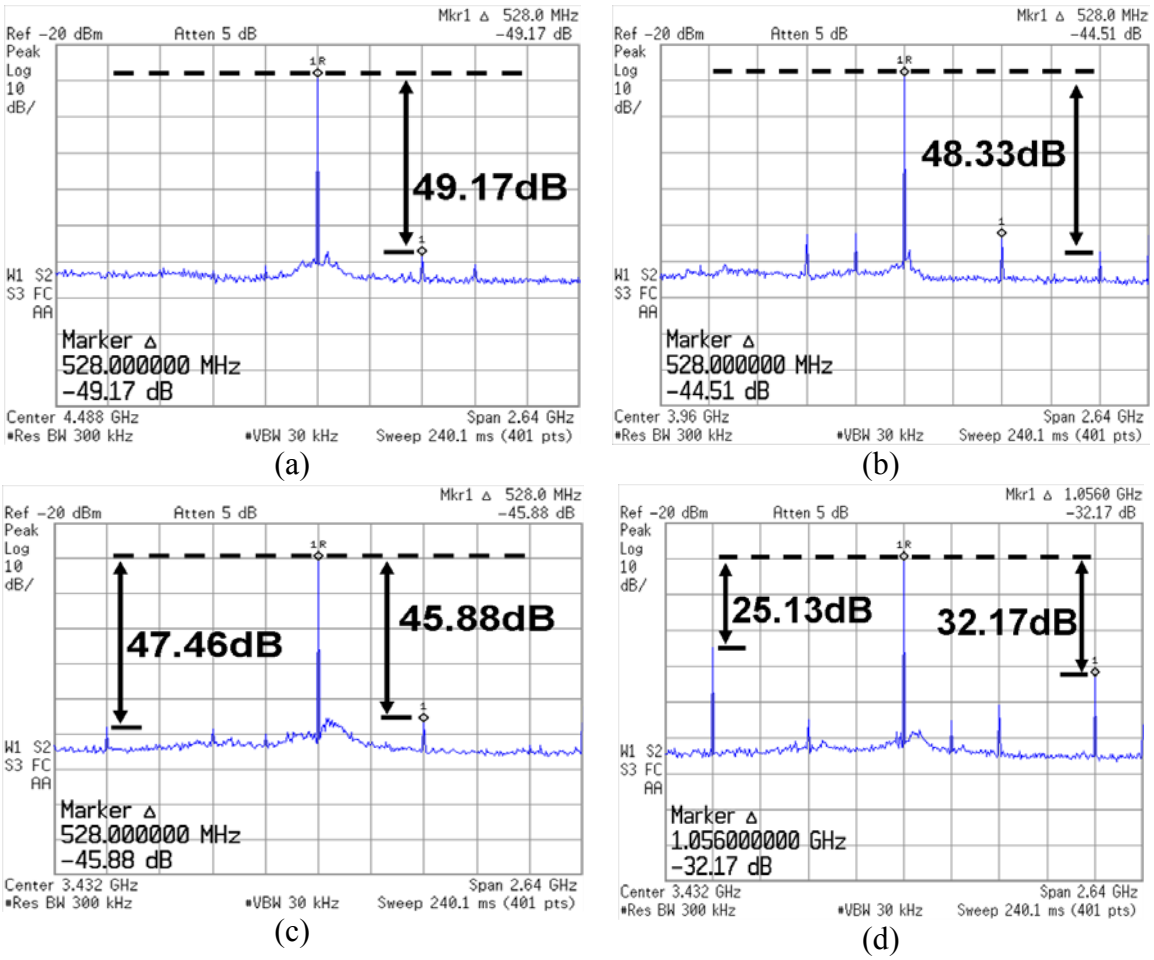


Figure 3.23: Measured spectrum of (a) band 3 with SSPG on. (b) Band 2 with SSPG on. (c) Band 1 with SSPG on. (d) Band 1 with SSPG off.

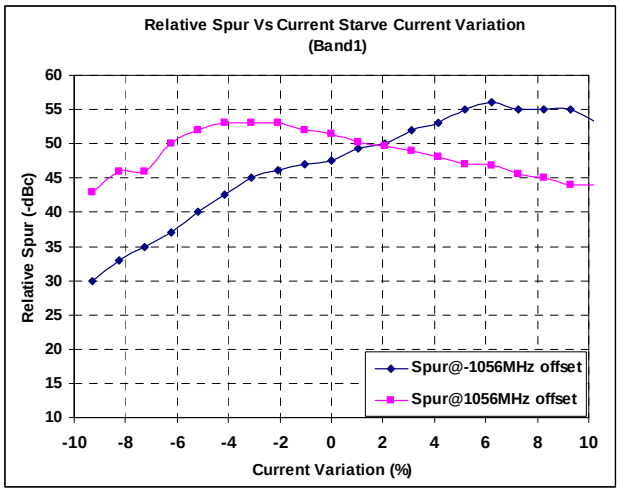
The pulse shaping reduces the spurs at 1056 MHz offset by 22 dB and suppresses them to below -47 dBc. These spurs fall in 2.4 and 5 GHz bands where strong interferers from IEEE802.11a/b/g are expected. Therefore, the proposed technique improves the spectral purity of ILO-based synthesizer which allows co-existence between UWB and ISM users. The in-band spurs observed at 528 MHz offset are due to even harmonics which are supposed to be eliminated through differential operation. In the measurement, it is observed that the balun employed to create differential reference signal for SSPG has phase imbalance larger than the duty cycle error introduced by our circuit. This will

increase the pulse width imbalance error discussed earlier and results in higher even harmonics observed at the output. Nevertheless, the worst case spurious tones are below -45, -44 and -49 dBc in band 1, 2 and 3 respectively. As these spurs do not fall within ISM bands, their requirements are much relaxed and they should be below -35 dBc as shown in section 3.2.1.

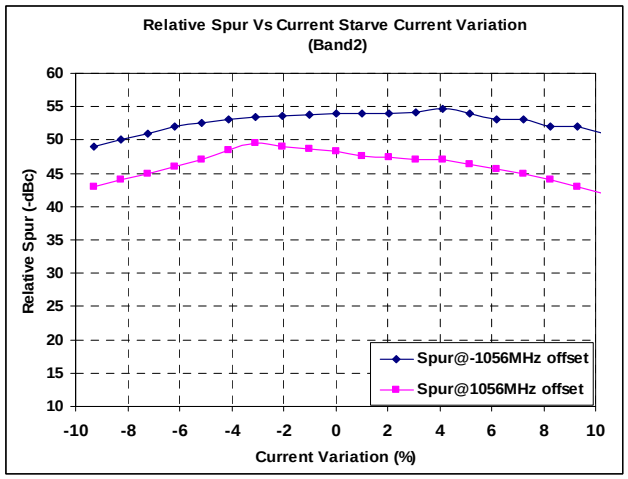
Fig. 3.24(a)-(c) show the sensitivity of the spur reduction to variation in the current of the starved inverters on the delay line. As can be seen, ±3.3% variation in the current can be tolerated while achieving spur level of better than -45 dBc. To identify the effect of mismatch, the spur performance is also measured on 5 chips and is shown in Table 3.1. All chips meet the requirement of the WiMedia-UWB, which indicates the effectiveness and robustness of the proposed circuit techniques.

Table 3.1: Measured Spur Suppression (dBc) for Different Chips.

Center Frequency (MHz)	**3432**		**3960**		**4488**	
Offset Frequency (MHz)	**-1056**	**1056**	**-1056**	**1056**	**-1056**	**1056**
Chip 1	**-47**	**-50**	**-54**	**-48**	**-58**	**-56**
Chip 2	**-45**	**-52**	**-53**	**-47**	**-58**	**-58**
Chip 3	**-46**	**-53**	**-54**	**-46**	**-58**	**-57**
Chip 4	**-49**	**-49**	**-53**	**-46**	**-56**	**-55**
Chip 5	**-45**	**-53**	**-55**	**-48**	**-59**	**-58**



(a)



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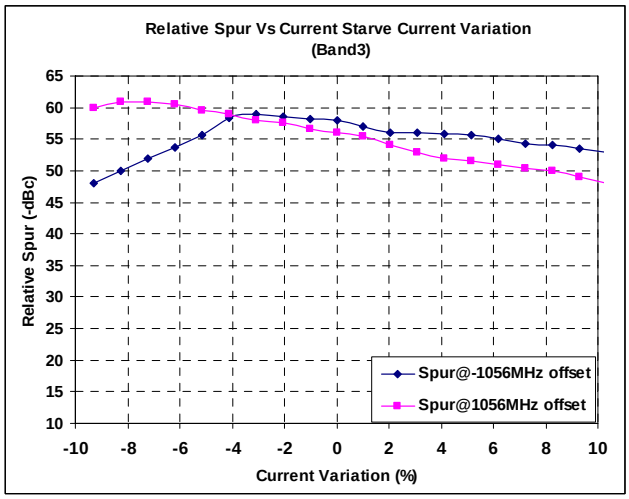


(c)

Figure 3.24: Measured spur level with variation of the current of the starved inverters. (a) Band 1. (b) Band 2. (c) Band 3.

Table 3.2 summarizes the performance of the prototype and compares it with state-of-the-art designs. This work achieves the lowest reported spurs among all ILO-based UWB synthesizers validating the effectiveness of the pulse shaping. It achieves similar spur performance as SSB mixer technique with 2× lower power and 7× smaller area. The higher power consumption compared to [33] is a general power-area trade-off which arises from the method of quadrature generation.

Table 3.2: Performance Summary.

	ISSCC05 [40]	JSSC06 [39]	ISSCC08 [44]	ISSCC08 [34]	JSSC11 [33]	This work
Number of Bands	3	7	14	3	3	3
Technique	SSB Mixer	SSB Mixer	SSB Mixer	ILO	ILO	ILO
In-band spurs(dBc)	-35	-37	-33	-19	-31	-44
Out-of-band spurs(dBc)	-45	-48	<-45	-	-32	-47
Phase Noise (dBc/Hz) @1MHz	-104	-103	-98	-112	-114	-122
Settling time (ns)	1	1	3.3	4	2.44	4.7
Power Diss.(mW)$^{+}$	73.5	48	117	36	14.5	21.6
Supply Voltage(V)	2.7	2.2	1.8	1.2	1.2	1.2
Active Area(mm^2)	1.1	1.43	5.5	0.074	0.27	0.15
Technology	0.25-um SiGe	0.18-um CMOS	0.18-um CMOS	90-nm CMOS	0.13-um SiGe BiCMOS*	0.13-um CMOS
FOM	20.69	27.08	11.18	13.51	26	36.94

$^{+}$Only [40] uses on-chip crystal oscillator for input reference. All the others use external reference of at least 264 MHz.
*Only CMOS used.

In order to have a comparison between different designs, a figure of merit (FOM) is proposed to include different performance factors other than power and spurs. The FOM is given by

$$FOM = 10\log(\frac{N}{P_{diss}.A.t_s}\frac{P_{Carrier}}{P_{Spur}}) \quad (3.25)$$

where P_{diss} is the power dissipation in mW, A is the active die area in mm^2, $P_{Spur}/P_{Carrier}$ is the worst case relative side band suppression in linear scale, N is the number of frequency bands covered, and t_s is the switching time. The FOM includes area as the representation of complexity used in the implementation (Area is mainly affected by the number of the inductors required in each design and is not easily scalable with technology). Number of bands is also included as it is generally more challenging to cover a wider frequency range. As can been seen in Table 3.2, this work shows 30% improvement in FOM along with low level of spurs compared to the state-of-the-art.

3.9 Chapter Summary

In this chapter, operation of sub-harmonic injection locked oscillators was discussed and it was shown that the sub-harmonic ILO is a viable substitute for traditional PLLs in fast hopping applications. However, they suffer from poor spectral purity which limits their capability in wide band applications such as WiMedia UWB. The requirements on synthesizer were established and a simplified analysis to mathematically estimate the level of spurious tones at output of sub-harmonic ILOs was presented. It was also shown that there is a direct trade-off between locking time and spectral purity. To relax this design trade-off, a pulse shaping technique was introduced which significantly improves the spurious tone without sacrificing the settling time of

ILO. The technique has been experimentally validated with test chips tailored to UWB application. The proposed technique can also be applied to other systems such as software-defined radios or frequency multipliers. The test chip achieves the in-band spur of -44 dBc and out-of-band spur of -47 dBc which is the best spur among reported ILO-based UWB synthesizers in the literature. In addition, detailed analysis on the achievable spur reduction due to the impact of circuit non-idealities was performed. This analysis provides guidelines for circuit design and matching requirement.

Chapter 4

Low-Power RF Transmitter Based on Injection Locking

4.1 Introduction

With the recent development of wireless biomedical applications such as wireless capsule endoscopy and neural recordings, there has been an increasing demand for low-power high-data rate transmitters. The ultra-low power radio required for these applications have several characteristics. First, these applications are characterized by asymmetric high-data rate up-link and low-data rate down-link. The desired *on-body* transceiver requires a low-power high-data rate transmitter and a low-data rate receiver. Second, to further conserve energy and save battery life, the receiver needs to operate in the form of "sniffing" or "wake up" and the transmitter requires fast start-up time to exploit heavy duty cycling to maximize the energy efficiency. Even for biomedical

applications with low-data rate, it is usually recommended to buffer the data, transmit at the highest possible data rate and exploit duty cycling. This technique will reduce the average current consumption and time window for interference [54]. It should be pointed out that the small batteries used in these devices usually exhibit large internal impedance. This limits the amount of peak current it can support without significant output voltage variation. Thus, the peak power of the radio must also be minimized in order to be powered by these small batteries. Finally, minimum form factor is an important consideration and thus minimum external component count is desirable to reduce the bill of material and physical size.

Although low-power low-data rate wake-up receiver with decent performance has been reported [55-57], it remains a challenge to achieve transmitter capable of tens of Mbps in sub-mW range. Currently reported ultra-low power transmitters [31, 58-66] trade off spectral efficiency for energy efficiency and employ frequency-shift-keying (FSK) or on-off-keying (OOK) modulations to simplify the transmitter architecture and reduce the power consumption. However, these modulation schemes limit the data rate to a few Mbps and are not suitable for applications like capsule endoscopy or neural recording. Here we provide two examples to gain insight on the desired data rate. For capsule endoscopy, given a color depth of 8 bits/pixel, a frame size of 640×480, a frame rate of 6 fps and RGB color scheme, the required raw data rate is in the proximity of 44 Mbps. For neural recording with sampling rate of 15 kS/s and 10 bits of resolution, data rate for typical 256 channels approaches 32 Mbps.

In theory, QPSK doubles the bandwidth efficiency of OOK and quadruples the bandwidth efficiency of FSK [67]. Therefore, QPSK modulation scheme has recently emerged as a promising candidates for these high data rate applications [68], [69]. A phase-mux based transmitter is reported in [68]. However, the need of phase-locked loop and *LC* voltage controlled oscillator operating at twice the desired output frequency incur both power and area penalties. Moreover, long start-up time of the PLL limits the transmitter duty cycling capability and energy conservation. The transmitter in [69] exploits the output phase versus free running frequency characteristic of an injection locked *LC* oscillator for multiphase generation. However, calibration of the switched capacitor bank for reasonable error vector magnitude (EVM) is non-trivial and requires a complicated calibration loop with large area overhead. An interesting point to note is that both architectures employ *LC* oscillators. However, given that the optimum operation frequency for on-body devices is below 1 GHz [63], *LC* oscillators that operates at such low frequencies require significant chip area [68, 69] or several off-chip inductors [59, 60].

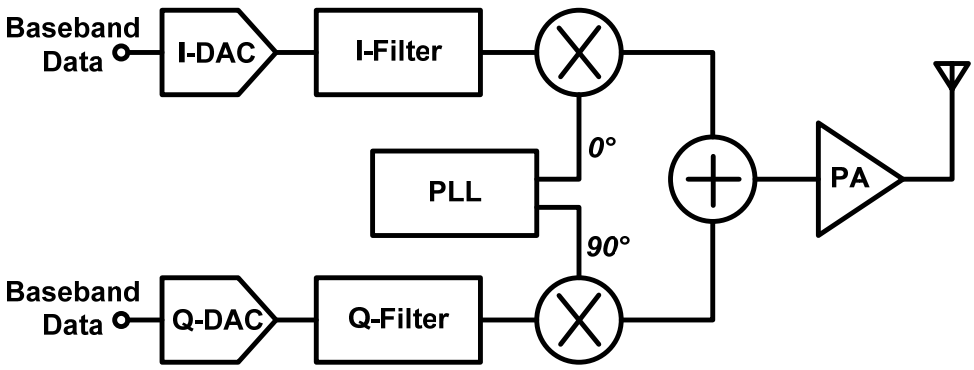
This chapter presents a highly digital 915 MHz ISM band transmitter with data rate of 55 Mbps. We simplify the transmitter architecture significantly by making use of injection locked ring oscillator and digital PA. This leads to the proposed transmitter that provides spectral efficient 8PSK or O-QPSK modulations and obtain an energy efficiency of 15.5 pJ/bit which is the lowest reported to date. The proposed architecture also eliminates the use of PLL with slow settling time and achieves start-up time of shorter than 80 ns.

4.2 Architecture

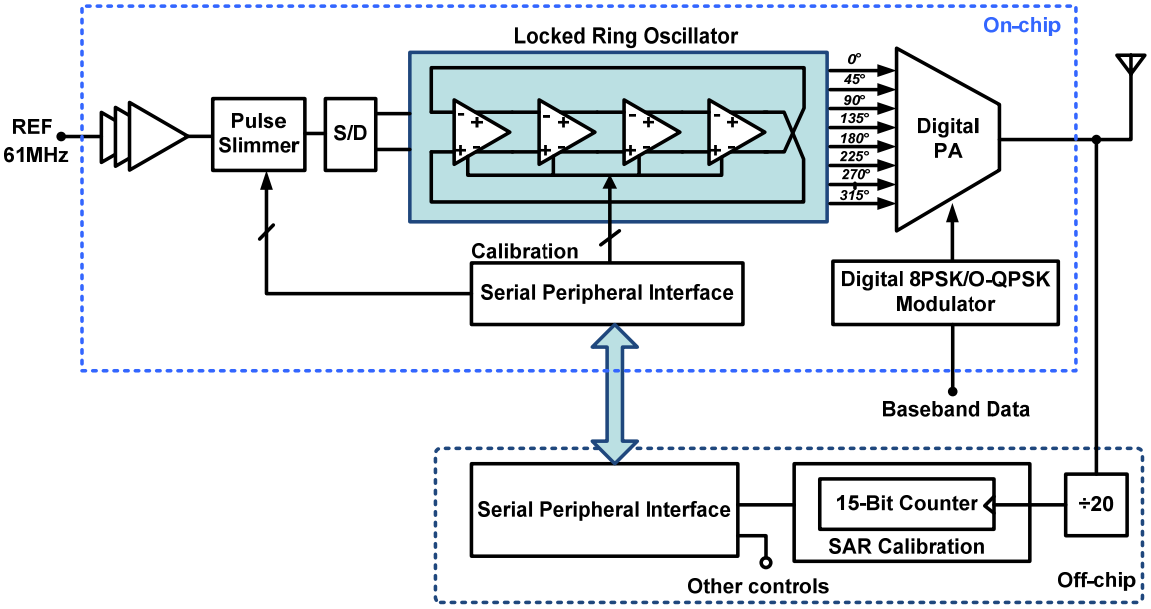
Conventional direct up-conversion transmitters (Fig. 4.1(a)) for quadrature modulations typically contains two digital-to-analog converters (DAC), two filters, quadrature mixers, a PLL and a power amplifier (PA). This architecture has several disadvantages for use in low power biomedical systems. Firstly, the required output power of PA for such applications is generally low to avoid over heating of the body tissue. Therefore, the carrier generation block (such as PLL) normally dominates the power dissipation and determines the transmitter efficiency. This is the main reason why most transmitters reported for biomedical application avoid using PLL and adopt free running oscillator [58, 59]. Secondly, the long PLL settling time prohibits duty cycling to maximize energy conservation. Thirdly, large device sizes required to overcome I/Q path mismatch and offset do not favor low power implementation. Finally, high speed DACs and wide-band filters required for high data rate are usually achieved at the expense of larger power.

It was shown in chapter 2 and 3 that an oscillator locks to the N^{th} harmonic of an injection signal if the free running frequency of the oscillator is close to that harmonic. This sub-harmonic locking phenomenon causes the oscillator output frequency to become N times the injection signal frequency. In fact, a sub-harmonic injection-locked system behaves like an integer-N frequency synthesizer without a need for any phase detector, divider and loop filter. Therefore, it can provide a compact, low-power and low-noise solution for frequency synthesis with extremely fast transient response as validated by

measured results in chapter 3. Here, we use a sub harmonic injection-locked oscillator to replace the PLL and facilitate the carrier generation as shown in Fig. 4.1(b).



(a)



(b)

Figure 4.1: (a) Conventional direct conversion transmitter architecture. (b) Proposed architecture.

In addition, multiphase generation required for phase shift keying (PSK) modulation is easily obtained through the use of a four stage differential ring oscillator (RO). Although RO normally suffers from poor phase noise and frequency instability compared to *LC* oscillator, this issue is solved by injection locking of the oscillator to the 15^{th} harmonic of a 61 MHz crystal reference as mentioned before. Therefore, the resulting carrier generation block is simplified which leads to significant area and power saving.

Multiple phases of the carrier generated by the ring oscillator will then drive a digital PA. Here we take the advantage of digitally controlled power amplifier to embed phase selection based on modulated data into the PA. A low frequency digital 8PSK/O-QPSK modulator directly controls the PA to provide the modulated output to the antenna. Note that unlike conventional method, the proposed architecture is amenable to process and supply scaling due to its digital nature and can be easily ported to the newer technological nodes.

To compensate for process, voltage and temperature (PVT) variations, the free running frequency of the oscillator is calibrated off-line using a digital loop that determines the code word required for digitally controlled delay elements in the RO. The frequency of the ring is digitally measured by counting the ring cycles for a fixed period of time. A successive-approximation search algorithm is then used to adjust the delay code. It will be worth noting that this transmitter is intended to work in-vivo and therefore the temperature variations are small which abates the need for frequent

frequency calibration. The frequency resolution depends on many factors which will be discussed in the next sections.

4.3 Transmitter Performance Consideration

The performance of the proposed architecture depends on many factors such as accuracy of the phase generated by multiphase generator, mismatches, and phase noise. In general, the performance of the transmitter is characterized by EVM of its transmitting signal. Although the proposed architecture is more robust to analog impairments due to its highly digital nature, its performance may still be limited by circuit non-idealities. This section will discuss the design consideration for the proposed architecture and provide insights into the design of various building blocks.

4.3.1 Systematic Phase Error

Since ring oscillators do not have a single dominant frequency component, the frequency domain and phasor models do not apply for their analysis. Time domain delay based model has been used in [29, 70] to study the injection locking phenomena in ring oscillators. However that model only explains the ring oscillators with delay cells based on *RC*-loads and differential pairs, and does not apply well for current starved inverters. In this section, we will explain the locking mechanism in ring oscillators based on current starved inverters.

Fig.4.2(a) shows the behavioral model of such a ring oscillator. Each stage consists of a current source that upon crossing of $V_{DD}/2$ charges or discharges the

capacitive load. The clipper models the amplitude limiting behavior of the inverter. The propagation delay of each stage is the time that it takes for the output to reach to the transition point ($V_{DD}/2$) and can be calculated as $t_p = \frac{CV_{DD}}{2I}$. Therefore, the circuit will oscillate at the free running frequency of $f_0 = \frac{1}{T_0} = \frac{1}{2\times 4\times t_p}$ and each stage provides $\theta = \frac{2\pi t_p}{T_0} = \frac{\pi}{4}$ of delay.

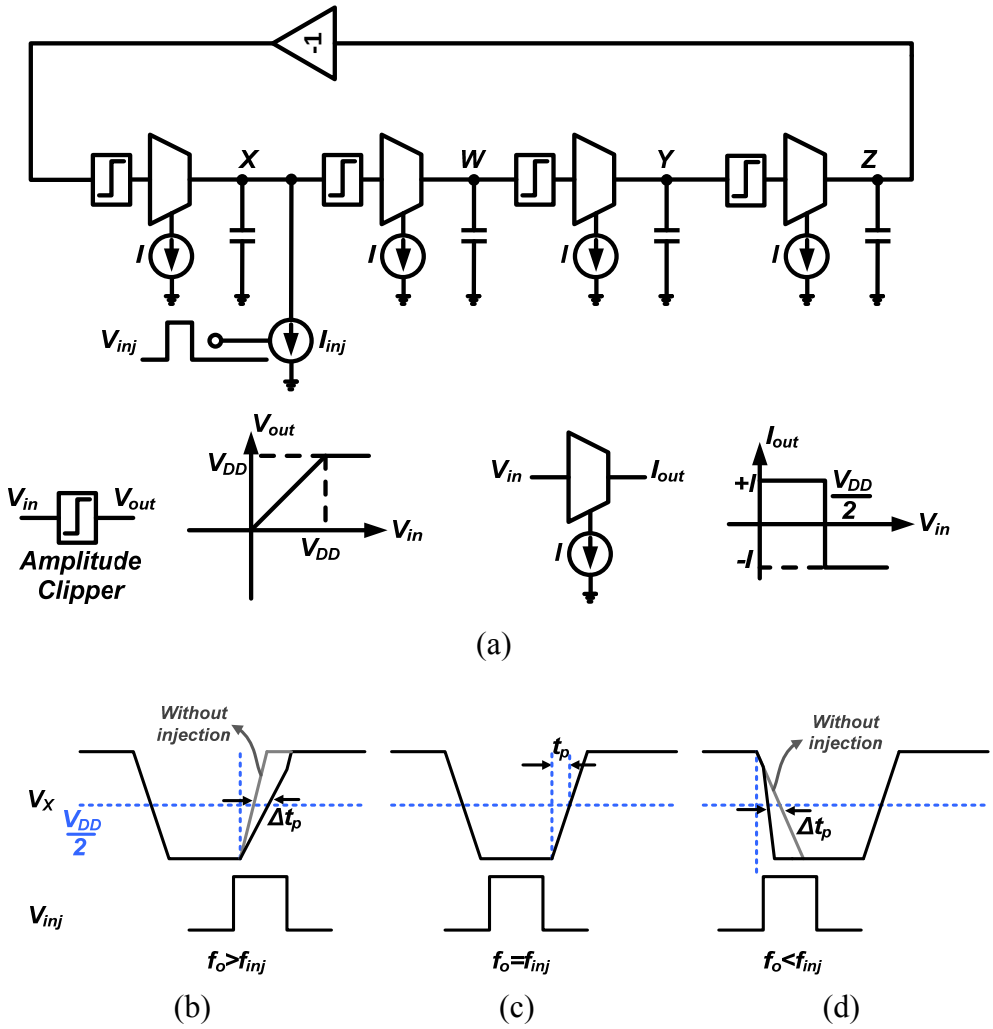


Figure 4.2: (a) Model of injection-locked ring oscillator with current starved inverter delay cells. Voltage of node X and injection voltage for (b) $f_0 > f_{inj}$. (c) $f_0 = f_{inj}$. (d) $f_0 < f_{inj}$.

Now, suppose a synchronization signal V_{inj} at f_{inj} turns on the additional current source I_{inj} to discharge the capacitive load at node *X*. Let us first consider the fundamental locking ($f_{inj} \approx f_0$) to understand how such a current source can change the frequency of the oscillator from f_0 to f_{inj} . If $f_{inj} = f_0$ (Fig.4.2(c)), at steady state, there will be no delay between the oscillator and injection signal and therefore the additional current is injected into the node *X* only when the voltage is saturated at node *X* and it will not cause any change in the delay of this stage. If $f_{inj} < f_0$ (Fig.4.2(b)), there will be a delay between injected and output signal. I_{inj} discharges the capacitor at node *X* while *I* is charging the capacitor. Therefore, the total net current that charges the capacitor is reduced and increases the delay in this stage. This increase in the delay of the first stage, increases the period of the output to $T_{out} = 7t_p + t_p + \Delta t_p = T_{inj} = \frac{1}{f_{inj}}$ and locks the oscillator to the injected signal. If $f_{inj} > f_0$ (Fig.4.2(d)), I_{inj} discharges the capacitor at node *X* while *I* is discharging the capacitor. Therefore, the total net current that discharges the capacitor is increased and decreases the delay in this stage. This decrease in the delay of the first stage, decreases the period of the output to $T_{out} = 7t_p + t_p - \Delta t_p = T_{inj} = \frac{1}{f_{inj}}$ and locks the oscillator to the injected signal. Therefore, only one stage modulates the total delay around the loop which causes error in the generated output phases. For example, the delay between *Y* and *Z* will be

$$\theta = \frac{2\pi t_p}{T_{inj}} = \frac{2\pi}{T_{inj}} \cdot \frac{1}{8f_0} = \frac{\pi}{4}\frac{f_{inj}}{f_0} = \frac{\pi}{4} + \frac{\pi}{4}\left(\frac{f_{inj} - f_0}{f_0}\right) \qquad (4.1)$$

Therefore the relative phase error between the two stages is proportional to the frequency offset between the injection signal and free running oscillator:

$$\theta_{error} = \frac{\pi}{4}\left(\frac{f_{inj} - f_0}{f_0}\right) = \frac{\pi}{4}\left(\frac{\Delta f}{f_0}\right) \qquad (4.2)$$

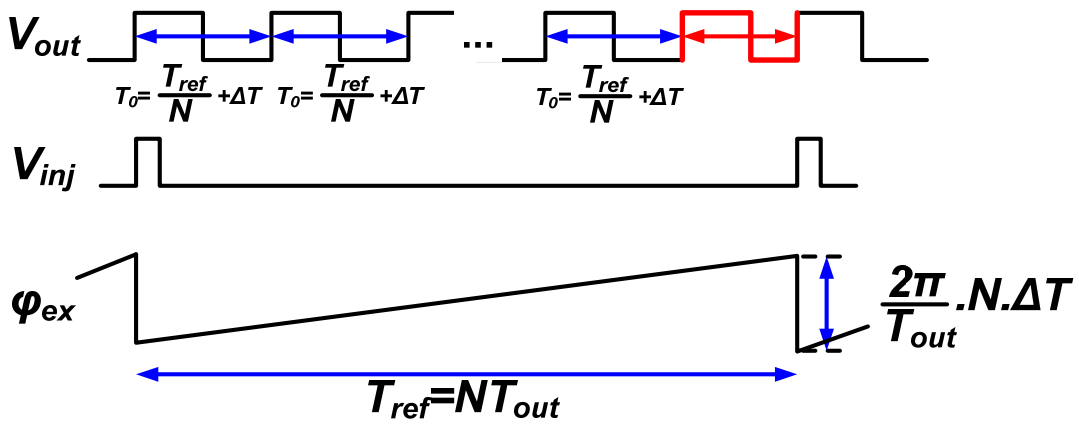
In sub-harmonic injection locking, if the self-resonant frequency of ring oscillator differs from that of the N^{th} harmonic of the injection signal, the injection signal will correct the oscillator frequency by introducing Δt_p in the first output cycle of the ring oscillator. As there is no injection signal for the subsequent N-1 output cycle, the ring oscillator will oscillate with its free running frequency (Fig.4.3(a)). If the N^{th} harmonic of the injection signal frequency is close enough to the free running frequency to "lock" the oscillator, such a periodic correction of the output phase can be consider as a phase modulation (PM) in the output. Focusing only on the fundamental harmonic, the output can be written as:

$$V_{out} \approx V_0 \cos(\omega_{out} t + \varphi_{ex}(t)) \qquad (4.3)$$

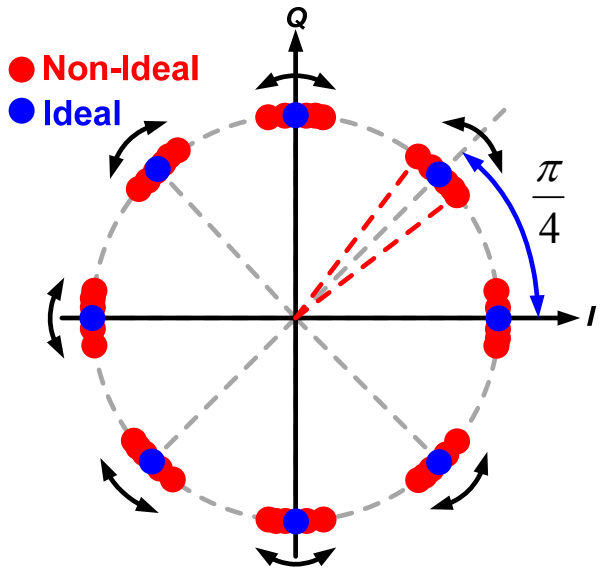
where $\omega_{out} = 2\pi N f_{ref}$ and $\varphi_{ex}(t)$ is the saw tooth waveform shown in Fig.4.3(a) which causes PM modulation. This modulation causes a variation of the phase around the ideal symbol reference point as shown in Fig.4.3(b). The RMS phase error will be:

$$\begin{aligned} \theta_{error,rms} &= \sqrt{\frac{1}{T_{ref}} \int_{T_{ref}} (\varphi_{ex}(t))^2 \, dt} \\ &= \frac{2\pi}{T_{out}} \cdot \frac{N.\Delta T}{\sqrt{3}} = \frac{2\pi.N.\Delta f}{\sqrt{3} f_0} \end{aligned} \qquad (4.4)$$

where $\Delta T = T_0 - \frac{T_{ref}}{N}$ and $\Delta f = f_{inj} - f_0 = N f_{ref} - f_0$.



(a)



(b)

Figure 4.3: (a) Behavior of sub-harmonic injection locked oscillator when $f_0 \neq N.f_{ref}$. (b) Effect of PM on the constellation.

For small phase errors (and assuming negligible amplitude error), EVM is mainly dominated by the phase errors:

$$EVM \approx \theta_{error,rms} \qquad (4.5)$$

In case of a digitally controlled ring oscillator, the required frequency resolution for the oscillator can be calculated based on the targeted EVM (required BER) using (4.4) and (4.5). Therefore the above equations help determine the specification for the frequency resolution required for the oscillator.

From frequency domain perspective, this periodic disturbance in the output of the oscillator generates spurs. This observation has been reported in [71] and it has been discussed that the frequency offset between free running and injection frequency causes misalignment between the injection and free running VCO edges and therefore causes spurs. However no mathematical expression is provided to estimate the level of spurs based on the frequency offset. Here we provide an approximation for spur level based on the above analysis. Substituting $\varphi_{ex}(t)$ in (4.3) by its Fourier expansion and focusing only on the fundamental harmonic of it:

$$V_{out} \approx V_0 \cos(\omega_{out} t - \frac{2N\Delta T}{T_{out}} \sin(\omega_{ref} t) - \cdots) \qquad (4.6)$$

simplifying (4.6) results in:

$$V_{out} \approx V_0 \cos(\omega_{out} t) \cos(\frac{2N\Delta T}{T_{out}} \sin(\omega_{ref} t)) + V_0 \sin(\omega_{out} t) \sin(\frac{2N\Delta T}{T_{out}} \sin(\omega_{ref} t))$$

$$\approx V_0 \cos(\omega_{out} t) + V_0 \frac{2N\Delta T}{T_{out}} \sin(\omega_{out} t) \sin(\omega_{ref} t) \qquad (4.7)$$

By rearranging (4.7) we obtain

$$V_{out} \approx V_0 \cos(\omega_{out} t) + V_0 \frac{N\Delta T}{T_{out}} [\cos((\omega_{out} - \omega_{ref})t) - \cos((\omega_{out} + \omega_{ref})t)] \qquad (4.8)$$

which shows the fundamental output along with two side bands at $\pm \omega_{ref}$. Therefore,

$$Spur(dBc) = 20\log(\frac{N\Delta T}{T_{out}}) \quad (4.9)$$

Considering $\Delta T = \frac{1}{f_0} - \frac{1}{f_{out}} = \frac{1}{f_0} - \frac{1}{Nf_{ref}}$, the spurs can be expressed in terms of frequency error by

$$Spur(dBc) = 20\log(N \cdot \frac{|f_{out} - f_0|}{f_0}) = 20\log(N \cdot \left|\frac{\Delta f}{f_0}\right|) \quad (4.10)$$

we will verify (4.10) against measured results in section 4.5.

4.3.2 Random Phase Error

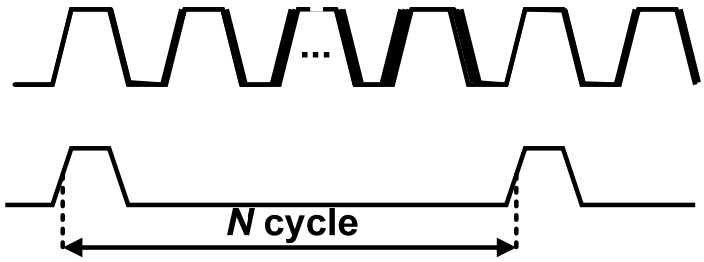
There are two sources of random phase error that affects the performance of the transmitter:

A. Phase Noise

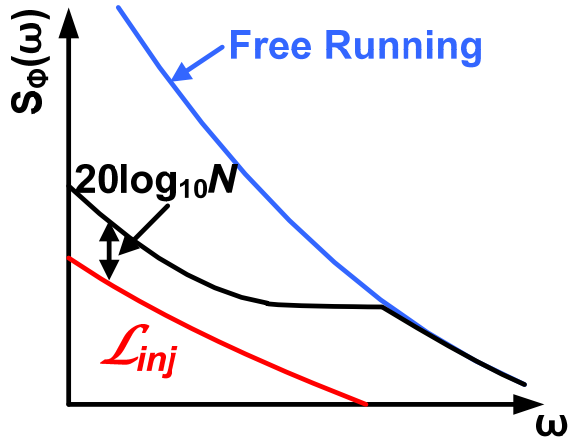
Phase noise of the injection locked oscillator or similarly phase realigned ring oscillators has been subject of research for many years and is well studied [19, 25, 71]. Here, we just provide some intuitive understanding and refer the reader to the above references for phase noise study.

From the time domain perspective, jitter in a free running oscillator accumulates over time, resulting in a drift of the phase in time. If we are multiplying the reference signal by *N*, the injection locking corrects the zero crossing of the oscillator every *N* period, thereby lowering the accumulation of jitter (see Fig.4.4(a)). It has been shown in [72] that the phase noise inside locking range would be constrained to $\mathcal{L}_{inj}$+20log*N*,

where $\mathcal{L}_{inj}$ is the phase noise of the sub-rate injection signal (If the free running frequency is close to the injected harmonic frequency).



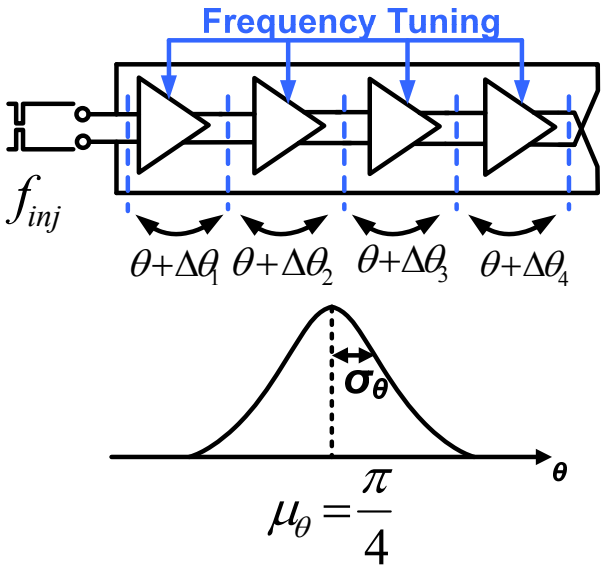
(a)



(b)

Figure 4.4: Effect of injection locking on oscillator in (a) Time domain perspective. (b) Frequency domain perspective.

Therefore, as can be seen in Fig.4.4(b), injection locking of the RO to a crystal reference can significantly improve its phase noise and is thus used in the proposed architecture. The effect of phase noise on the constellation is similar to PM modulation and the required phase noise to achieve a certain EVM can be obtained by calculating the total integrated jitter of the VCO and (4.5).



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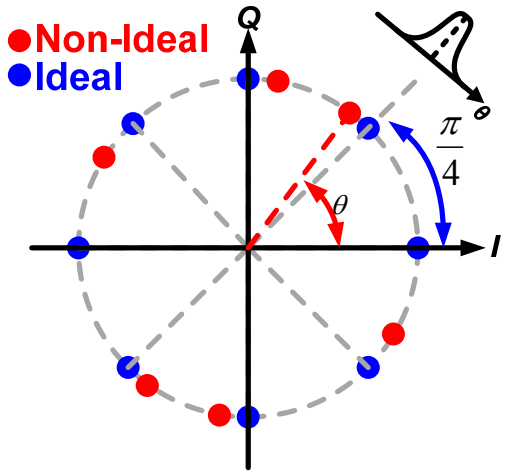


(b)

Figure 4.5: Random mismatch between delay cells in the oscillator. (b) Effect of random phase mismatch on the constellation.

B. Random Mismatch

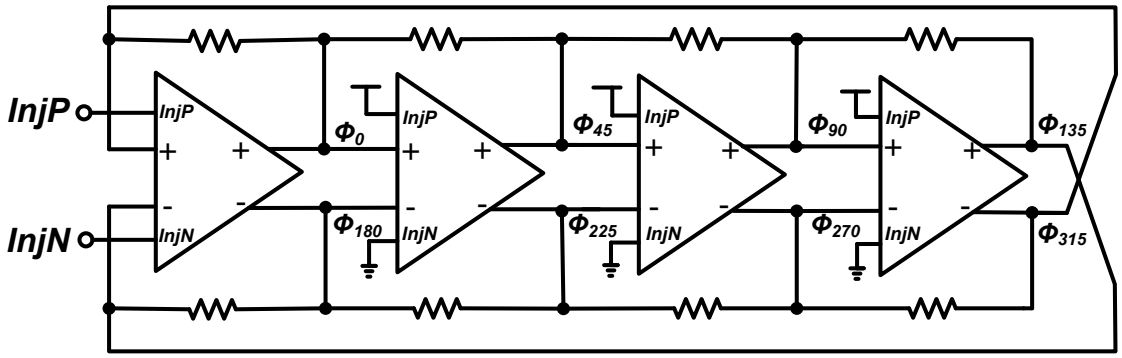
Let us assume a perfect oscillator without phase noise that is oscillating at $f_0 = f_{inj} = N.f_{ref}$. Further assume that the errors we discussed earlier do not exist. However, due to mismatch between delay cells, phase difference introduced by one stage can be different from another stage. Therefore each stage provides a mean phase step

of $\pi/4$ with standard deviation of σ_θ as shown in Fig.4.5(a). This error manifests itself as a distortion of the constellation as shown in Fig.4.5(b). In this work, this error is minimized by proper sizing of the delay cells and a circuit technique which will be discussed in the next section.

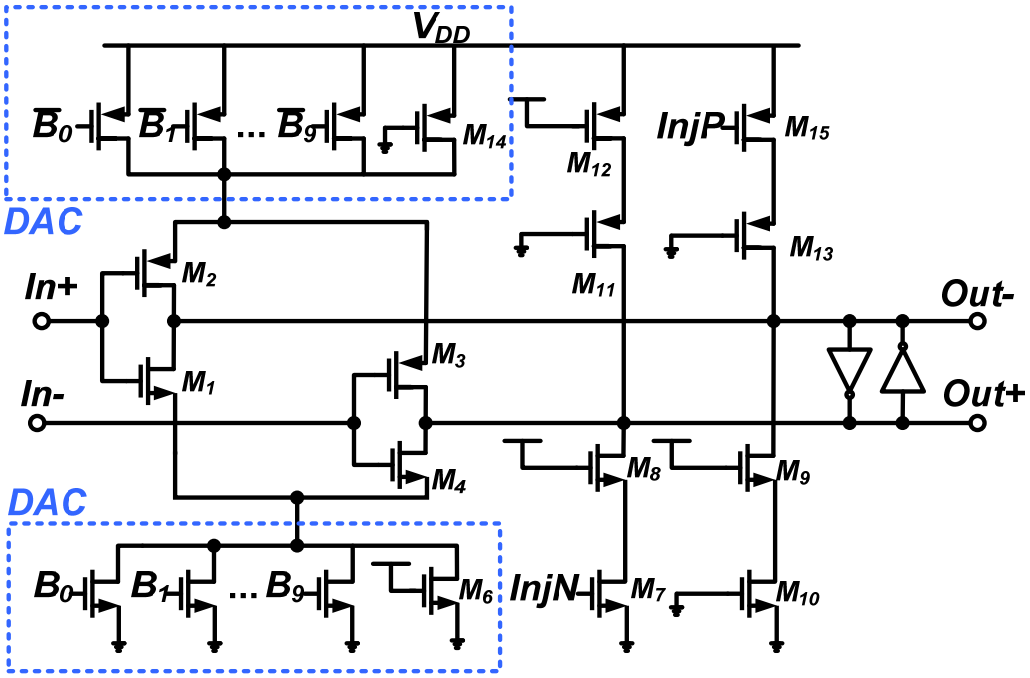
4.4 Circuit Implementation

4.4.1 Injection Locked Ring Oscillator

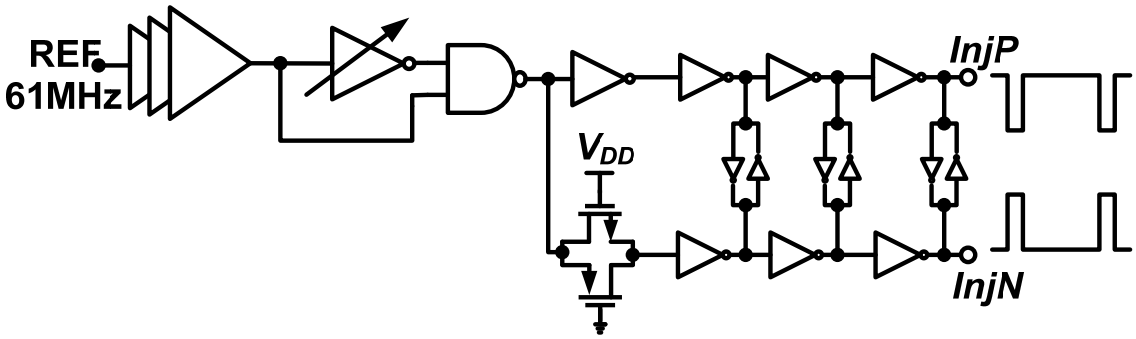
Shown in Fig.4.6(a), this prototype uses a 4-stage current starved pseudo-differential ring oscillator, which naturally provides eight phases of the carrier. Differential implementation also improves common-mode noise rejection. Although the reference pulse is injected only in the first stage of the ring oscillator, all other stages use the same cell to maintain matching. Detailed implementation of each delay cell is shown in Fig.4.6(b). The ratio between M_7-M_6 and M_{15}-M_{14} determines the injection ratio while M_8 and M_{13} replicate M_1 to M_4. The advantage of using this method is that the injection ratio is relatively insensitive to PVT variations. Moreover, M_9-M_{12} are added as dummies to balance the loading in the differential path. As shown in Fig.4.6(b), the oscillator is digitally controlled by two current DACs. Each DAC consists of 10-bit binary weighted array to cover the desired operation frequency range across the process corners. The frequency tuning resolution is set by the maximum acceptable PM and the required EVM based on (4.4) and (4.5). In this work, to minimize the deterministic source of phase error, the frequency resolution is designed to be less that 0.2 MHz in the worst case which is equivalent to a phase error of less than 0.4°.



(a)



(b)



(c)

Figure 4.6: Implementation of injection-locked ring oscillator. (b) Detailed schematic of the delay cell. (c) Pulse generator.

The pulse slimmer circuit shown in Fig.4.6(c) ensures that the width of the injection pulse is shorter than half the period of the oscillation of ring oscillator. Three-stage buffer with cross-coupled inverters minimizes the skew between the pulses and maintains the alignment in all process corners.

The accuracy of the 8 phases generated by the ring oscillator will impact the transmitter performance. Hence the propagation delay of each stage should be matched as closely as possible. In order to reduce the effect of random mismatch (caused by random variation in transistor dimension, threshold voltage and routing parasitic mismatch), mismatch filtering resistors [73] are used as shown in Fig.4.6(a). Intuitively, since each node is coupled to the adjacent nodes by the resistors, the transition edges average out and any mismatch between delay cells is reduced. The previous circuit model discussed in section 4.3.1 [Fig.4.2(a)] can be used to explain the effect of resistors as illustrated Fig.4.7(a).

Using KCL, the effective current that charges/discharges the inter-stage capacitor can be derived as follows:

$$I_{effective}(t) = I(t) + \frac{\frac{V_{\theta+45^\circ}(t) + V_{\theta-45^\circ}(t)}{2} - V_\theta(t)}{R/2} \qquad (4.11)$$

The second term on the right hand side of (4.11) is provided by the resistors and tries to equalize the delay. For example, if I in one stage is higher than other stages and charges the node V_θ faster, the mean value of $V_{\theta+45^\circ}$ and $V_{\theta-45^\circ}$ is smaller than V_θ and provide a negative current that reduces the effective current (Fig.4.7(c)). According to Monte-Carlo

simulations, this technique improves the standard deviation of the phase mismatch by 4.7 times.

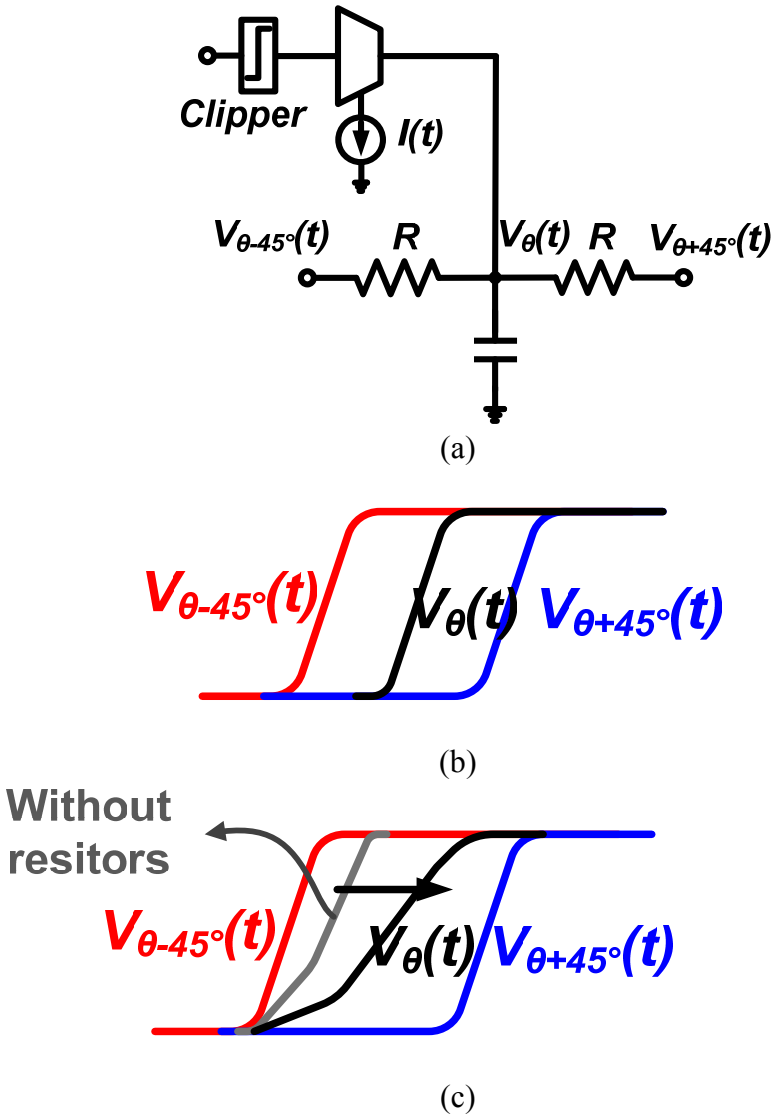


Figure 4.7: Effect of mismatch filtering resistors. (a) Simplified model. (b) Waveforms in the ideal case. (c) Waveforms in the presence of mismatch in current sources.

4.4.2 Digital Power Amplifier

Fig. 4.8 illustrates the digital PA with phase multiplexer circuit topology. It consists of 8 “unit” amplifiers. Each amplifier comprises two transistors in series. The

bottom transistors are driven by 8 different phases of the RF carrier, tapped from the ring oscillator. The cascode transistors act as switches controlled by the digital baseband modulator and select proper phases for each symbol. The combined output of all the amplifiers is connected to an off-chip matching network for impedance transformation to drive a 50-ohm antenna or a measurement equipment. One can either use all the unit amplifiers driven by an 8PSK modulator or only enable four of the unit amplifiers driven by a QPSK/O-QPSK modulator to obtain different modulation scheme. In this prototype, for testing flexibility, we have implemented two versions of this circuit, one for 8PSK modulation and one for O-QPSK.

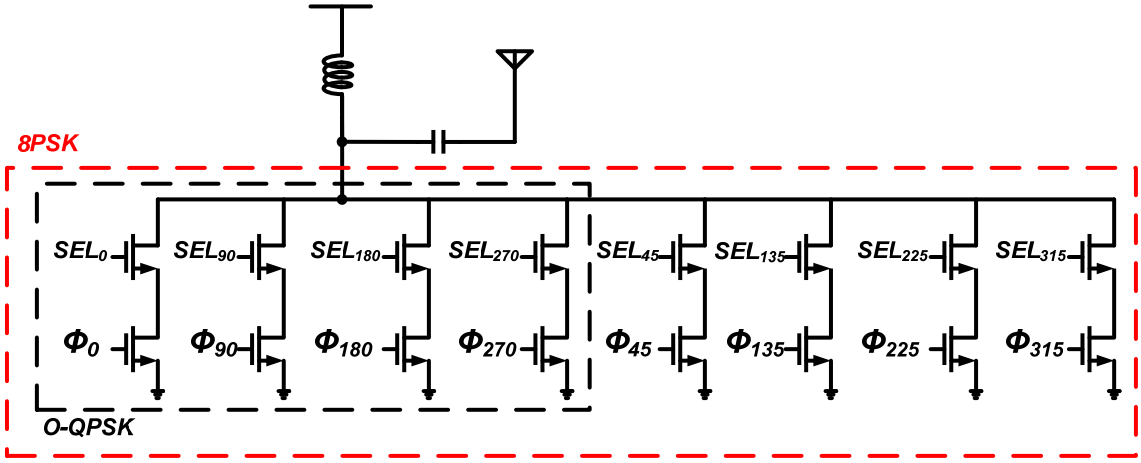


Figure 4.8: Digital power amplifier.

Mismatch between unit amplifiers comprising the digital PA can result in the output current mismatch. As shown in Fig. 4.9, this effect creates a distortion in the constellation and degrades the EVM. However, Monte-Carlo simulations show that by proper sizing of the unit amplifiers, matching of less than 1% can be easily achieved.

Therefore this error has minimal impact on the overall modulation quality of the transmitter.

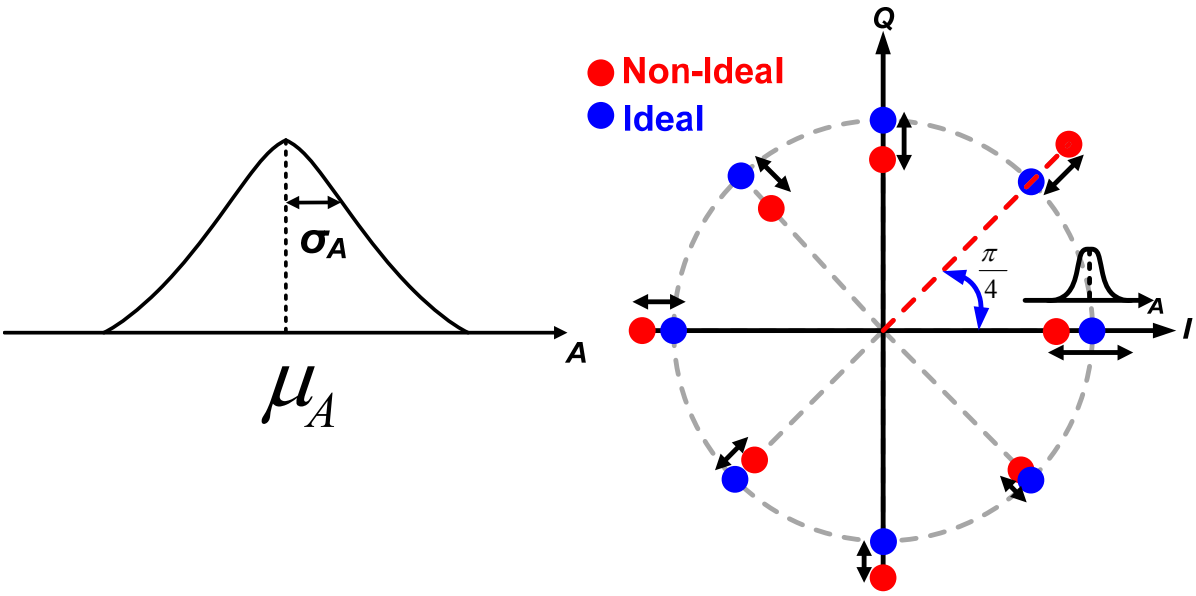


Figure 4.9: Effect of mismatch between units of power amplifier on the constellation.

4.4.3 Digital Baseband Modulator

Fig. 4.10 reveals the implementation of the baseband modulator. A programmable divide by 2/3 generates the sub-rate clock needed for serial to parallel converters. A 2-to-4 or 3-to-8 decoder is then used to drive the gate of the cascode transistors of the PA for O-QPSK and 8PSK mode respectively. Gray coding is obtained by proper connection (routing) between decoders and unit amplifiers in the PA. Moreover, the delay of the decoder is equalized in all the paths to minimize the skew between the output switching times. Such a skew might cause simultaneous conduction of unit amplifiers and thus introduce phase error and increase the settling time.

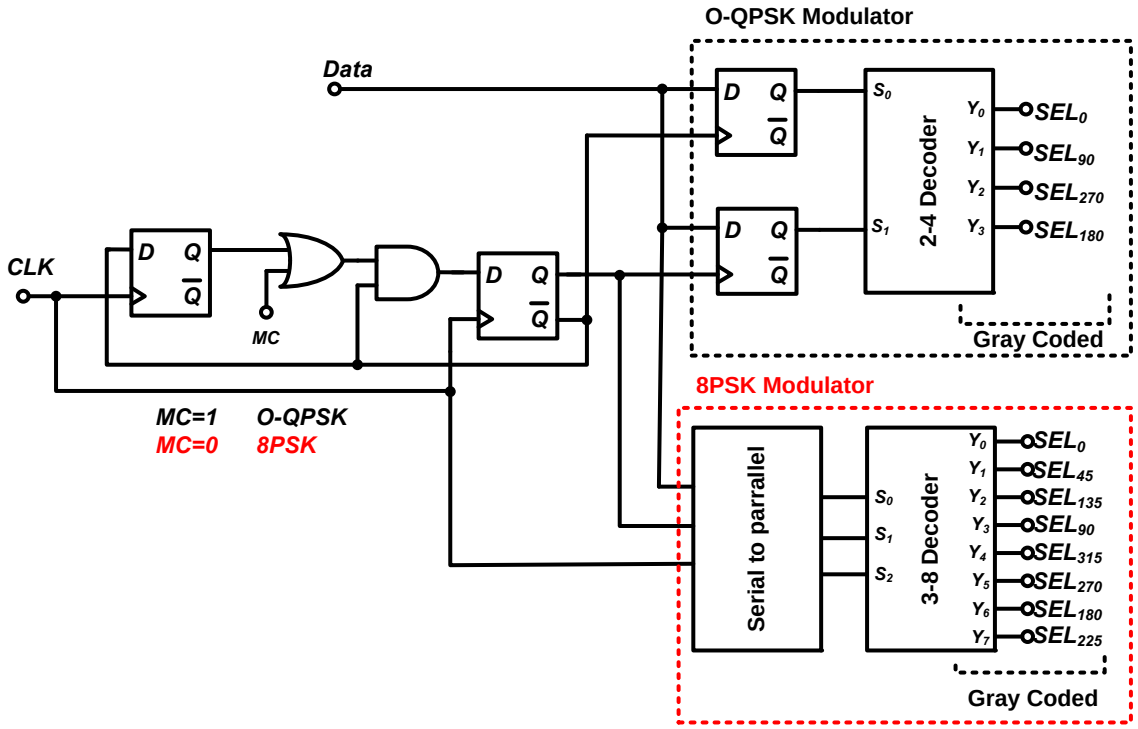


Figure 4.10: Digital baseband modulator.

4.5 Experimental Results

The 8PSK/O-QPSK transmitter is fabricated in 65 nm standard CMOS technology. Fig. 4.11 shows a micrograph of the die. Due to the highly digital nature of the architecture and the absence of area hungry PLL, the total active area is only 0.038 mm^2. The chip is packaged in Quad Flat No lead (QFN) and all the measurements have been performed on the packaged chips using a socket.

The ring oscillator can be tuned to oscillate from 758 to 950 MHz under 0.8-V supply. For the targeted output frequency of 915 MHz, the measured locking range of the oscillator extends from 902 to 927 MHz.

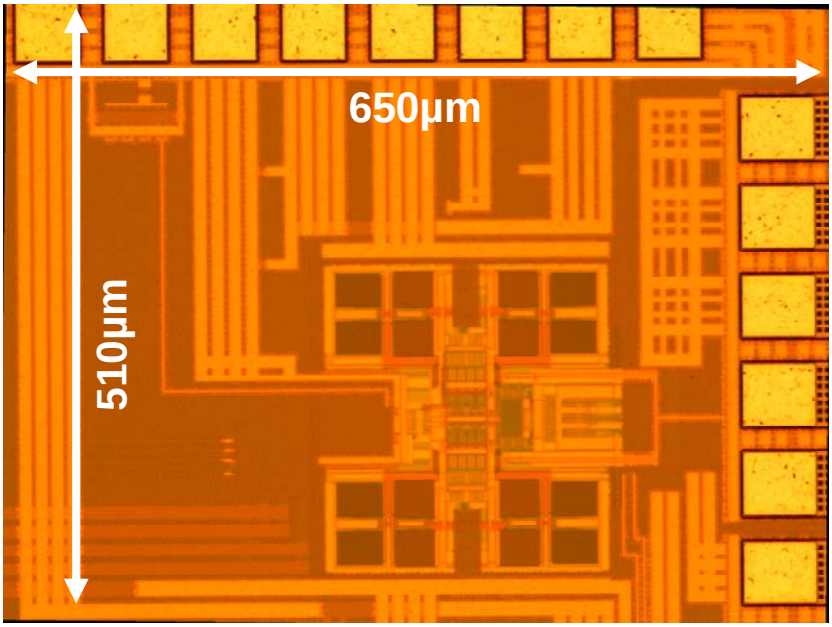


Figure 4.11: Die micrograph.

Measured phase noise of the ring oscillator in locked and unlocked condition is shown in Fig. 4.12. As illustrated, injection locking significantly improves the phase noise from 1 kHz to 1 MHz offset. In free running, the phase noise is -70 dBc/Hz at 200 KHz offset while under injection locking, it improves to -100 dBc/Hz at the same offset. Total integrated RMS jitter for the locked ring oscillator (from 1 kHz to 10 MHz) is 4.6ps or 1.52°.

Fig. 4.13 shows the output of the transmitter with -15 dBm output power. The output power can be increased up to -12 dBm. The unwanted spurious radiation outside the 915 MHz ISM band must be less than 500 μV/m field strength at 3 m distance or an EIRP of -41.2 dBm as stipulated by FCC [74]. The measured reference spur in our transmitter is less than -47 dBc or -62 dBm.

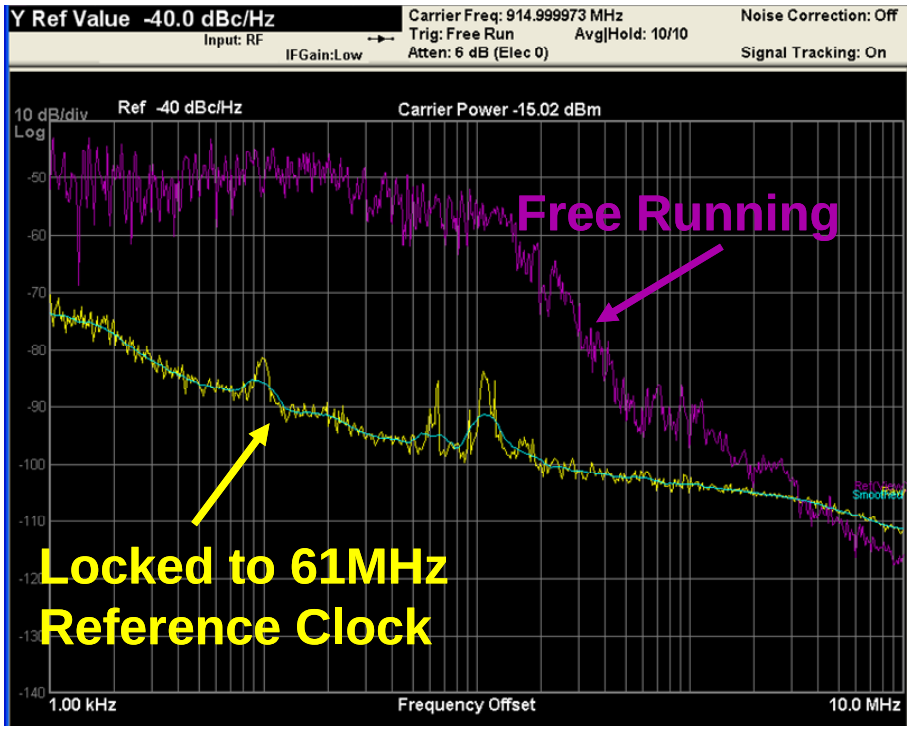


Figure 4.12: Measured phase noise of the ring oscillator under locked and unlocked condition.

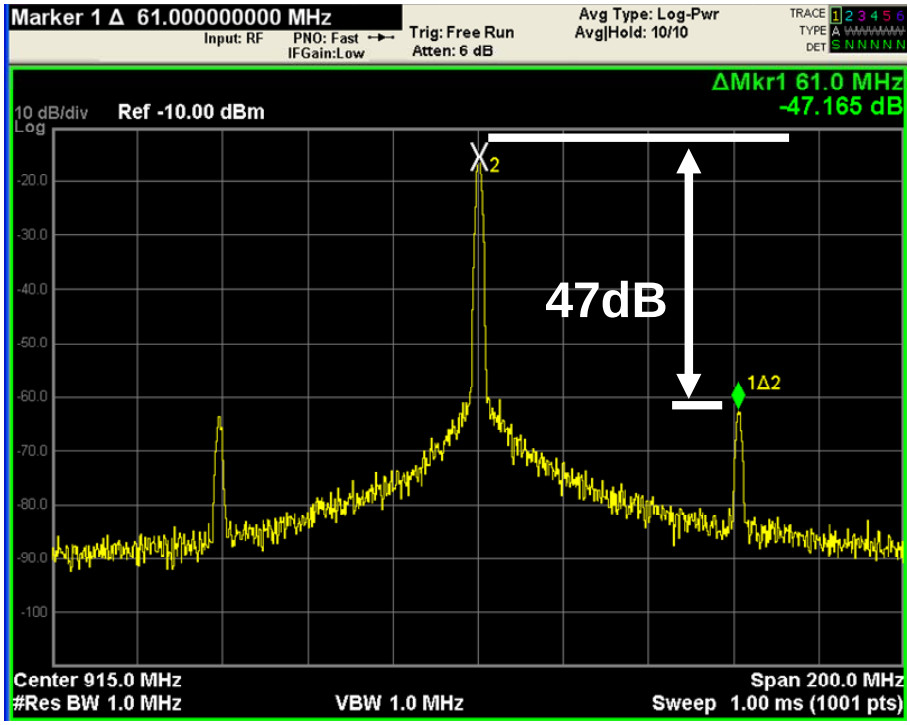


Figure 4.13: Measured output spectrum of the carrier at -15 dBm output power.

In order to verify (4.10), the spur level has been measured against different free running frequencies while the oscillator is locked to fixed frequency of 915 MHz. In addition, different reference frequency has been used to investigate the impact of multiplication ratio (N). As illustrated in Fig. 4.14, there is a very good agreement between estimation of (4.10) and measured results as well as Spectre-RF simulations. The slight deviation at very small frequency offsets between measurements and calculations might be due to insufficient isolation between reference and carrier or coupling through supply [71]. We verified this by disabling the injection buffer and observing that spurious tones at 61 MHz offset still exist around the free running spectrum. These spurs disappear when the 61 MHz reference is switched off, confirming that the coupling from reference to the output or supply of the ring oscillator is the culprit.

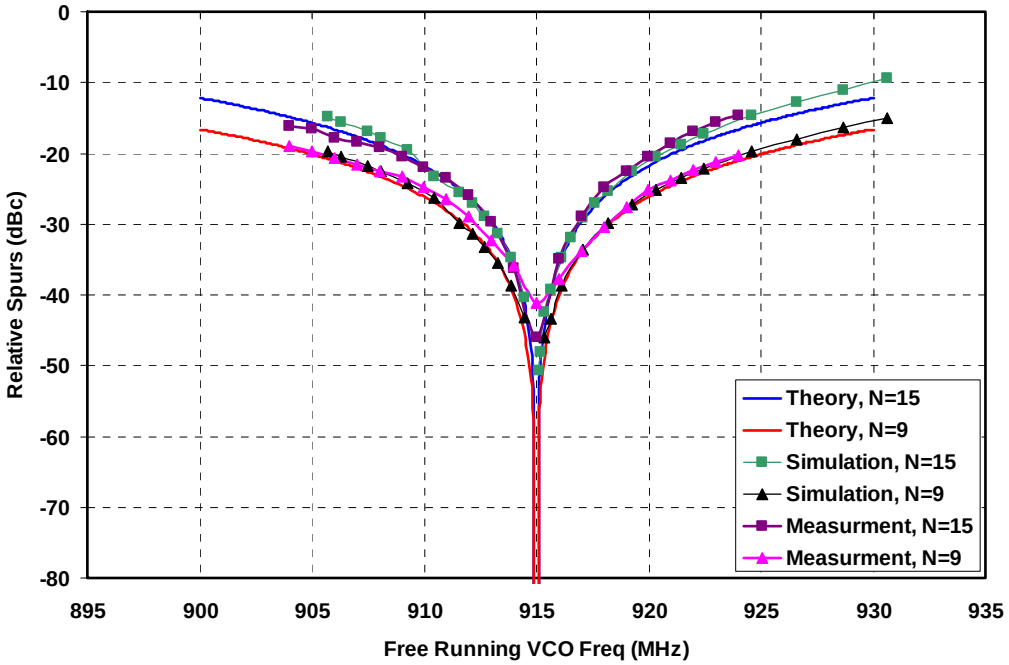


Figure 4.14: Theory verification of spur level estimation based on (4.10) for different N and offset frequency between free running and locking frequency.

Fig. 4.15 shows the measured start-up time of the injection locked ring oscillator which is shorter than 80 ns. This short settling time allows for more aggressive duty cycling of the transmitter to conserve more energy.

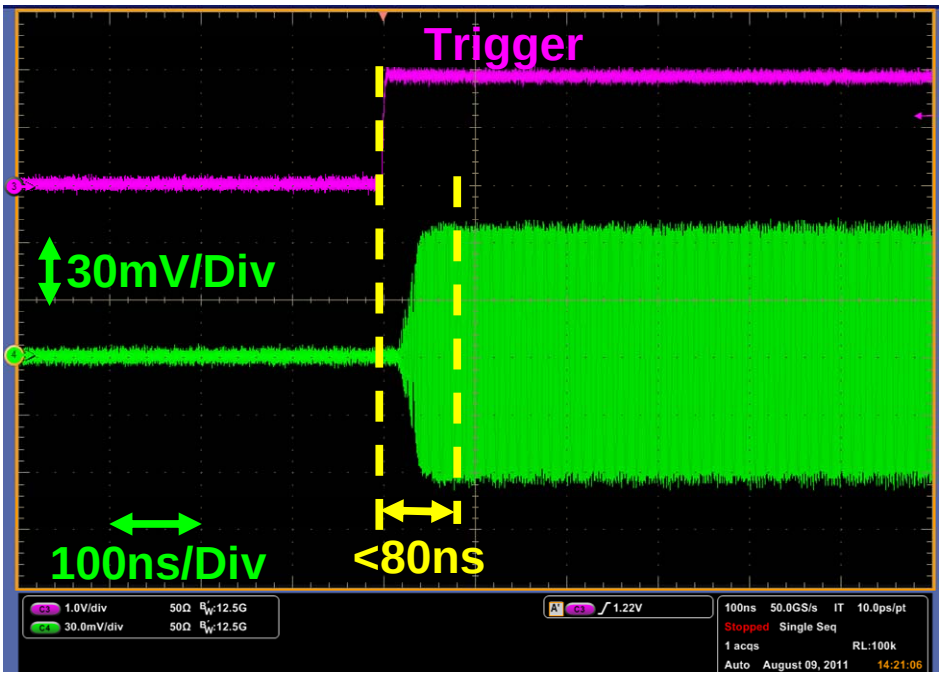


Figure 4.15: Measured settling time of the injection-locked ring oscillator with a step voltage on the supply.

Fig. 4.16 shows the measured constellation for 8PSK and O-QPSK mode. This measurement has been carried out on 10 chips to investigate the effect of mismatch. The worst case measured EVM at data rate of 55 Mbps are 3.8 and 4.46% respectively. This data rate is chosen to meet the ISM spectral mask. The maximum achievable data rate by the proposed transmitter is 90 Mbps with only slight deterioration in EVM to 4.77% and 6.88% for 8PSK and O-QPSK mode respectively. A typical 8PSK/O-QPSK receiver requires EVM of less than 15/23% to achieve bit error rate (BER) of less than 10^{-4} [75]. The measured EVM in our transmitter meets this requirement with a good margin.

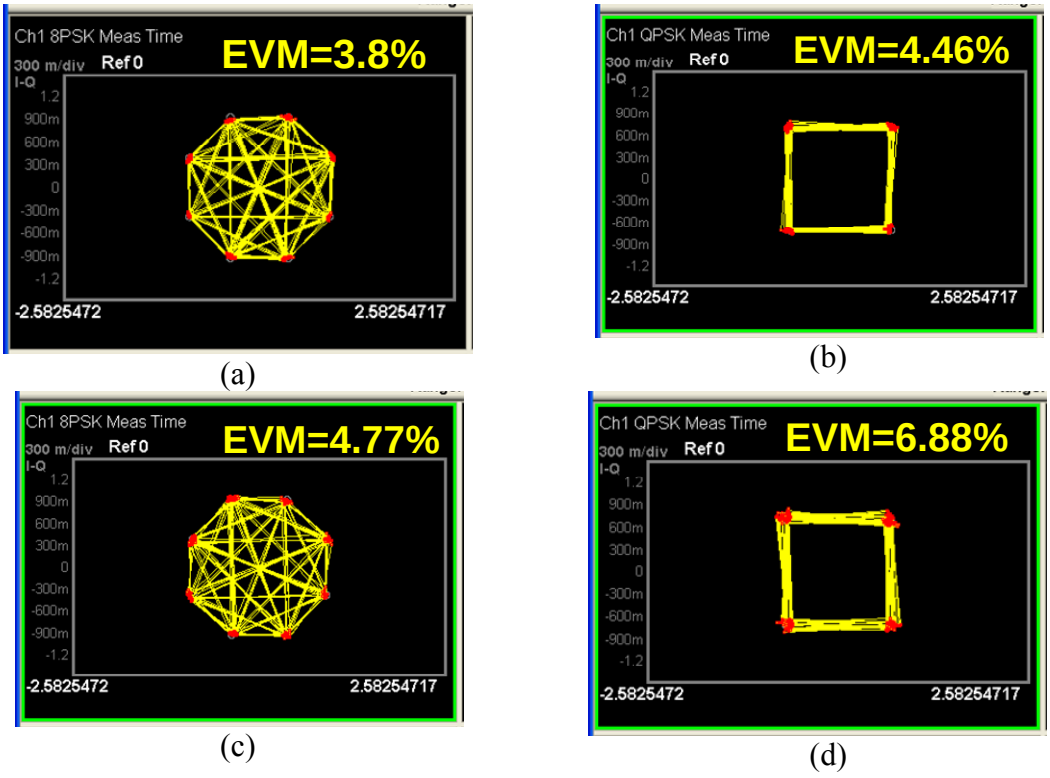


Figure 4.16: Measured constellation at (a) 8PSK at 55 Mbps. (b) O-QPSK at 55 Mbps. (c) 8PSK at 90 Mbps. (d) O-QPSK at 90 Mbps.

The ring oscillator consumes 538 μW and the PA consumes 286 μW while delivering -15 dBm output power. This figure has included the insertion losses of the socket, PCB and matching network. At 55 Mbps, 8PSK and O-QPSK digital modulators consume 13.8 μW and 10.7 μW respectively. The total power consumption in any mode of operation is less than 838 μW at 55 Mbps. For testing flexibility and to investigate spur performance in Fig. 4.14, the reference crystal oscillator is not included on chip in this design. However, simulations show that the crystal oscillator consumes only 15 μW which has minimal overhead on the total power consumption. (The crystal oscillator at similar frequency in [76] with two more ring oscillators locked to it consumes less than 22 μW in measurement.)

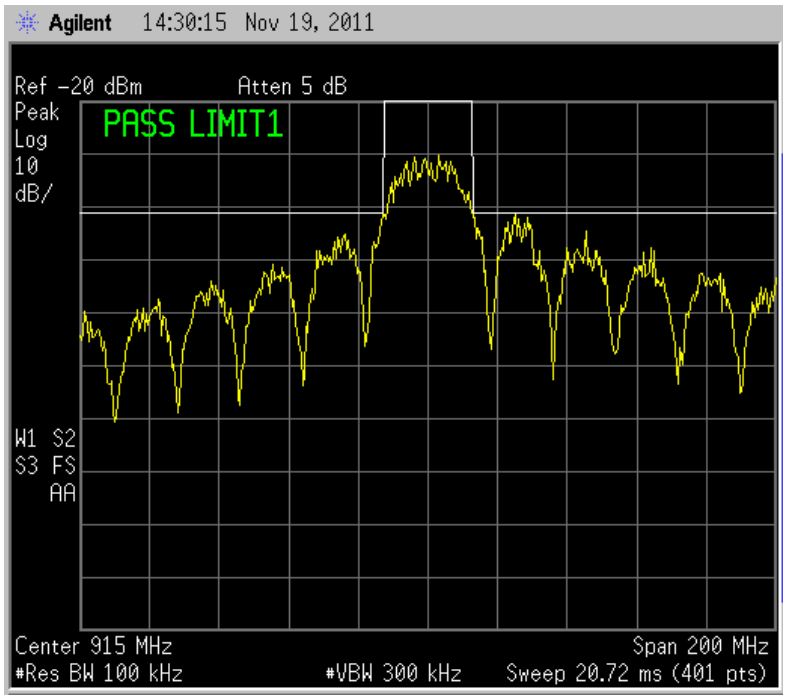


Figure 4.17: Measured output spectrum with output power of -15 dBm at 55 Mbps.

Fig. 4.17 shows the output spectrum for 8PSK mode at 55 Mbps. As stipulated by FCC regulation, medical devices operating at ISM band needs to meet the field strength of 50 mV/m at a distance of 3 m. Out of 902-928 MHz band, the field strength is 100 times smaller at the same distance [74]. This requirement translates to in-band mask of -1.23 dBm and out of band mask of -41.23 dBm (Measured with a resolution bandwidth of 100 kHz and wide video bandwidth). As illustrated, this prototype meets the FCC spectral mask and thus the interference to other wireless standard would not be a concern.

Table 4.1: Performance Summary and Comparison.

	[66] JSSC07	[61] ISSCC09	[62] ISSCC11	[68] CICC08	[60] JSSC11	This work
Frequency (MHz)	900	400	2400	400	920	915
Modulation	OOK	FSK	OOK	O-QPSK	FSK	8PSK or O-QPSK
Data Rate (Mbps)	1	0.1	10	15	5	55
Output power (dBm)	-11.4	-16	0	-15	-10	-15
Power Diss. (mW)	3.8	0.4	2.53	3.48	0.7	0.853*
Active Area (mm^2)	0.27	NA	0.882	0.7	1.65+	0.038
Energy/Bit (nJ/Bit)	3.8	4	0.253	0.23	0.14	0.0155
Supply Voltage (V)	0.8, 1, 1.4	1	1	1.2	0.7	0.8
Technology	0.18um	0.13um	90nm	0.18um	0.18um	65nm

***15μW added to account for crystal oscillator.**
+Chip area. It requires 4 off-chip inductors.

Table 4.1 summarizes the performance of the prototype and compares it with the state-of-the-art designs. To have a fair comparison, we have added 15 μW to the power consumption to account for the crystal oscillator. This work achieves the energy efficiency of 15.5 pJ/b (at 55 Mbps), which is 9× smaller than that of the state-of-the-art. It also has the lowest area without requiring any off-chip inductors (other than impedance matching network). This prototype is the first transmitter that provides spectral efficient 8PSK modulation with power consumption in sub-mW range, confirming the feasibility of achieving higher data rates with low power consumption. Fig. 4.18 places this work along with recently reported low-power transmitters for similar applications which shows a significant improvement in energy efficiency.

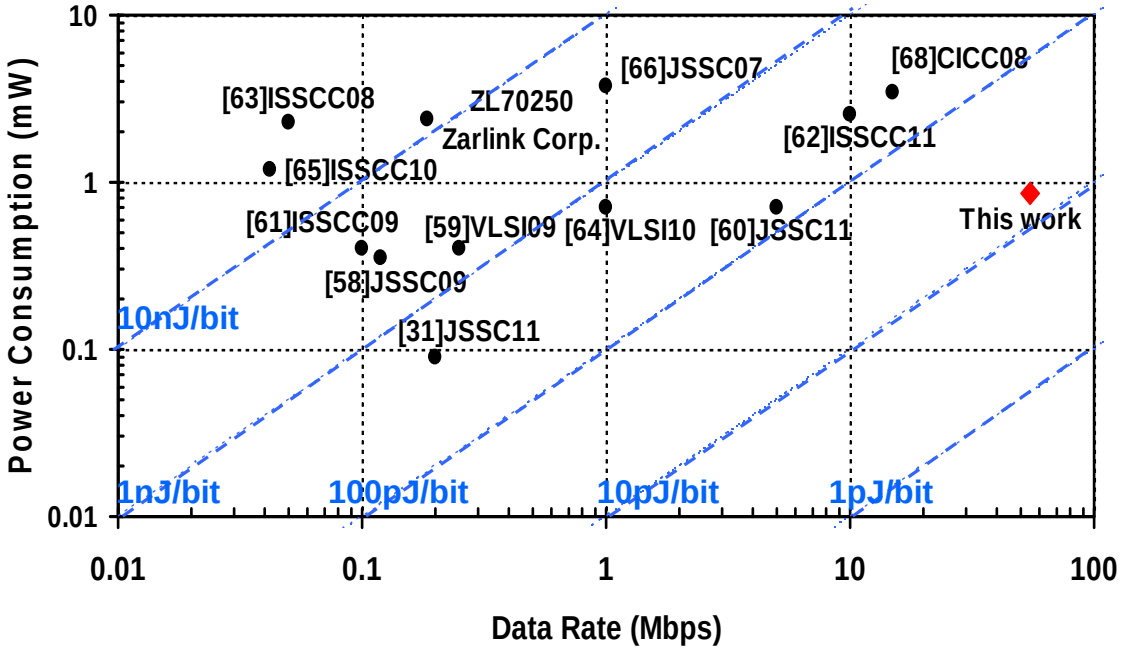


Figure 4.18: Energy efficiency comparison of low-power transmitters.

4.6 Chapter Summary

In this chapter special requirements of ultra low-power transmitter for biomedical applications are studied and state-of-the-art designs were reviewed. It was identified that currently reported transmitter trades off spectral efficiency for power efficiency and use OOK and FSK modulations which limits their data rate. To address this issue, new transmitter architecture based injection-locked ring oscillator and digital power amplifier is proposed. This architecture eliminates the need for slow and area hungry PLL which is the main reason for the poor efficiency of conventional approach. By reducing the power consumption in the carrier generation and using the spectral efficient modulation (8PSK/O-QPSK) to obtain higher data rates, our prototype is able to achieve energy efficiency of 15.5 pJ/b. which is the lowest among the state-of-the-art designs. In addition, detailed analysis on the spurious performance of the injection-locked frequency

multipliers is presented and a closed form formula for spur estimation is derived. Impact of circuit non-idealities on the transmitter performance is also discussed in depth which provides insight into circuit design.

Chapter 5

Conclusion

Continuing trends in the semiconductor industry requires communication devices that support higher data rates with an ever-growing demand for lower power consumption. This poses interesting challenges for many components of such devices. One of these key components in any communication device is frequency synthesizer. In this thesis, the concept of injection locking in oscillators has been used for frequency synthesis in order to achieve fast settling time while reducing the power consumption.

Fundamental principles of oscillators and phase noise are first introduced. A comprehensive theoretical understanding on operation of injection locking in both *LC* and ring oscillators is presented. Important characteristics of these circuits such as phase noise and transient behavior is investigated. Sub-harmonic injection locked oscillators are

identified to behave like first-order integer-N frequency synthesizer with very fast switching time.

Second, various frequency synthesizer architectures for ultra wide band were examined. Among them, injection locked synthesizers are recognized as promising candidates for low-power and small area implementation. However, poor spectral purity and high level of spurious tone in them are identified as their main limitations. A novel pulse shaping technique that reduces the spurious tones is proposed to address this limitation. Experimental results on the fabricated prototype in 0.13 μm CMOS shows 22 dB suppression in the spurious tones. A new approach to estimate the level of spurious tone in injection locked *LC*-oscillator is also developed. Moreover, detailed mathematical analysis on the achievable spur reduction due to the impact of circuit non-idealities was performed. The pulse shaping techniques developed in this dissertation can be used in many applications such as software defined radio or clock multiplication and deskew.

Third, different architectures for ultra-low power transmitters are explored. We identified that currently reported ultra-low-power transmitters trade off spectral efficiency to obtain energy efficiency and this limits their data rate to only a few Mbps which is not sufficient for high data rate applications. A new transmitter architecture based on injection locked ring oscillator and digital power amplifier is proposed to address this issue. The architecture described in this dissertation eliminates the need for slow and area hungry PLL. It also adopts spectral efficient 8PSK or O-QPSK modulations to obtain higher data rates. Fabricated prototype in 65 nm CMOS technology

achieved data rate of 55Mbps while consuming only 853 μW which translate to an energy efficiency of 15.5 pJ/bit. Apart from the above mentioned benefits, it is worth noting that unlike conventional method, the proposed architecture is amenable to process and supply scaling due to its digital intensive nature and can be easily ported to the newer technological nodes. Moreover, an analytical expression is derived to estimate the level of spurious tones in injection-locked ring oscillators and detailed analysis of the effect of circuit non-idealities on EVM of the transmitter output is provided.

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